Never stop thinking

32-Bit

Microcontroller

TC1782

32-Bit Single-Chip Microcontroller

Target Data Sheet/ACDC Target Specification

V 0.7 Preliminary 2010-03

Microcontrollers

Edition 2010-03

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1 Summary of Features

The **SAK-TC1782-320F180HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 180 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 180 MHz operation at full temperature range
- Multiple on-chip memories
  - 2.5 Mbyte Program Flash Memory (PFLASH) with ECC
  - 64 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One FlexRay™ module with 2 channels (E-Ray).

  - One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management
- 32 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

The **SAK-TC1782-256F133HL** has the following features:

- High-performance 32-bit super-scalar TriCore V1.3.1 CPU with 4-stage pipeline
  - Superior real-time performance
  - Strong bit handling
  - Fully integrated DSP capabilities
  - Single precision Floating Point Unit (FPU)
  - 133 MHz operation at full temperature range
- 32-bit Peripheral Control Processor with single cycle instruction (PCP2)
  - 16 Kbyte Parameter Memory (PRAM)
  - 32 Kbyte Code Memory (CMEM)
  - 133 MHz operation at full temperature range
- Multiple on-chip memories
  - 2 Mbyte Program Flash Memory (PFLASH) with ECC
  - 64 Kbyte Data Flash Memory (DFLASH) usable for EEPROM emulation
  - 128 Kbyte Data Memory (LDRAM)
  - Instruction Cache: up to 16 Kbyte (ICACHE, configurable)
  - 40 Kbyte Code Scratchpad Memory (SPRAM)
  - Data Cache: up to 4 Kbyte (DCACHE, configurable)
  - 8 Kbyte Overlay Memory (OVRAM)
  - 16 Kbyte BootROM (BROM)
- 16-Channel DMA Controller
- Sophisticated interrupt system with 2×255 hardware priority arbitration levels serviced by CPU or PCP2
- High performing on-chip bus structure
  - 64-bit Local Memory Buses between CPU, Flash and Data Memory
  - 32-bit System Peripheral Bus (SPB) for on-chip peripheral and functional units
  - One bus bridge (LFI Bridge)
- Versatile On-chip Peripheral Units
  - Two Asynchronous/Synchronous Serial Channels (ASC) with baud rate generator, parity, framing and overrun error detection
  - Three High-Speed Synchronous Serial Channels (SSC) with programmable data length and shift direction
  - One serial Micro Second Bus interface (MSC) for serial port expansion to external power devices
  - One High-Speed Micro Link interface (MLI) for serial inter-processor communication
  - One MultiCAN Module with 3 CAN nodes and 128 free assignable message objects for high efficiency data handling via FIFO buffering and gateway data transfer (one CAN node supports TTCAN functionality)
  - One General Purpose Timer Array Module (GPTA) with additional Local Timer Cell Array (LTCA2) providing a powerful set of digital signal filtering and timer functionality to realize autonomous and complex Input/Output management

- 32 analog input lines for ADC
  - 2 independent kernels (ADC0 and ADC1)
  - Analog supply voltage range from 3.3 V to 5 V (single supply)
- 4 different FADC input channels
  - channels with impedance control and overlaid with ADC1 inputs
  - Extreme fast conversion, 21 cycles of f_{FADC} clock
  - 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- 86 digital general purpose I/O lines (GPIO), 4 input lines
- Digital I/O ports with 3.3 V capability
- On-chip debug support for OCDS Level 1 (CPU, PCP, DMA, On Chip Bus)
- Dedicated Emulation Device chip available (TC1782ED)
  - multi-core debugging, real time tracing, and calibration
  - four/five wire JTAG (IEEE 1149.1) or two wire DAP (Device Access Port) interface
- Power Management System
- Clock Generation Unit with PLL

Ordering Information

The ordering code for Infineon microcontrollers provides an exact reference to the required product. This ordering code identifies:

- The derivative itself, i.e. its function set, the temperature range, and the supply voltage
- The package and the type of delivery.

For the available ordering codes for the TC1782 please refer to the **“Product Catalog Microcontrollers”**, which summarizes all available microcontroller variants.

This document describes the derivatives of the device.The **Table 1** enumerates these derivatives and summarizes the differences.

Table 1 TC1782 Derivative Synopsis

Derivative	Ambient Temperature Range
SAK-TC1782-320F180HL	T_A = -40°C to +125°C
SAK-TC1782-256F133HL	T_A = -40°C to +125°C

1 System Overview of the TC1782

The TC1782 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1782 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA Controller – DMA operations and interrupt servicing
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1782 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1782 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1782 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1782, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (LMB). Several I/O lines on the TC1782 ports are reserved for these peripheral units to communicate with the external world.

1.1 Block Diagrams

Figure 1 shows the block diagram of the **SAK-TC1782-320F180HL**.

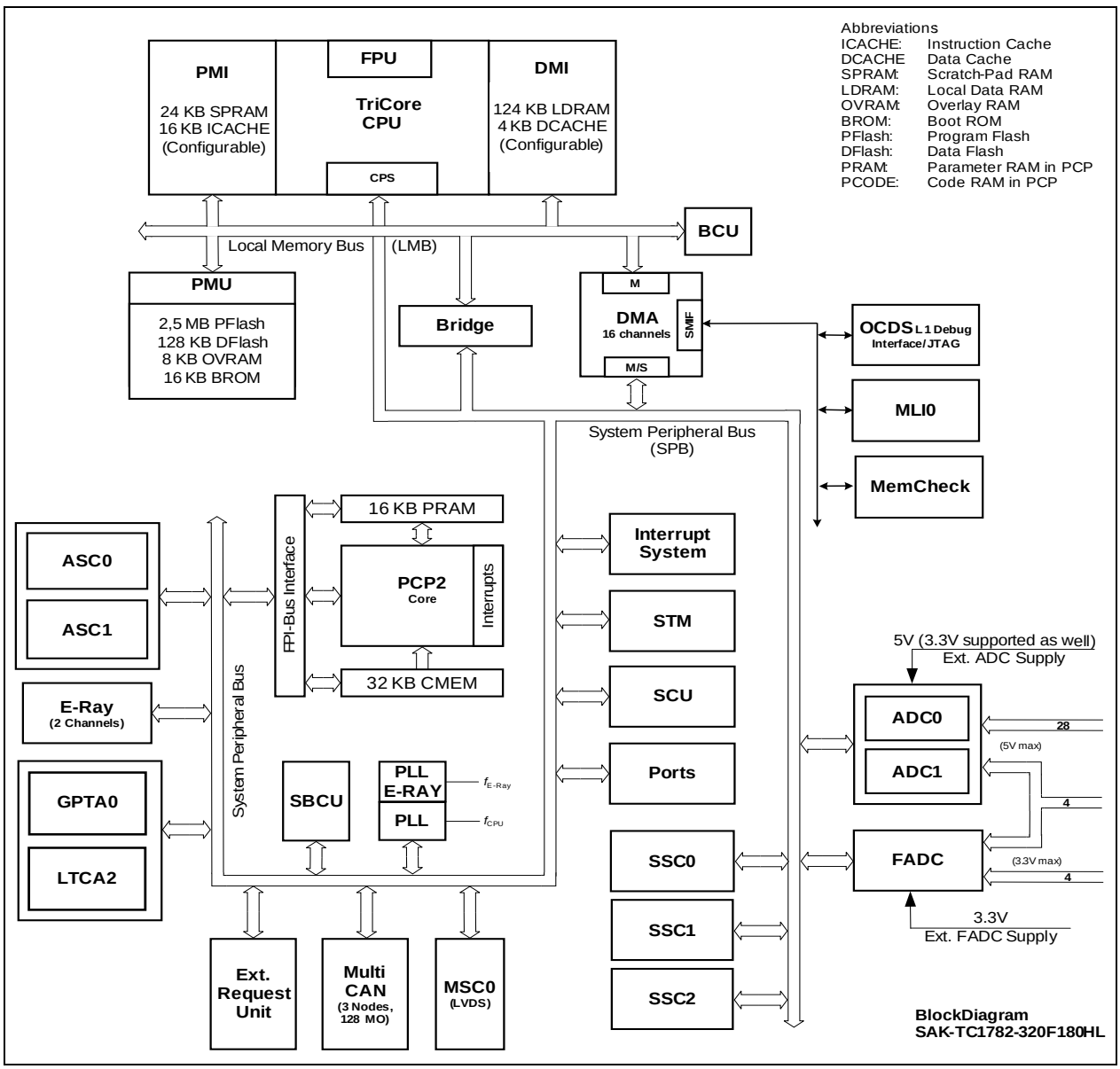


Figure 1 SAK-TC1782-320F180HL Block Diagram

Figure 1 shows the block diagram of the **SAK-TC1782-256F133HL**.

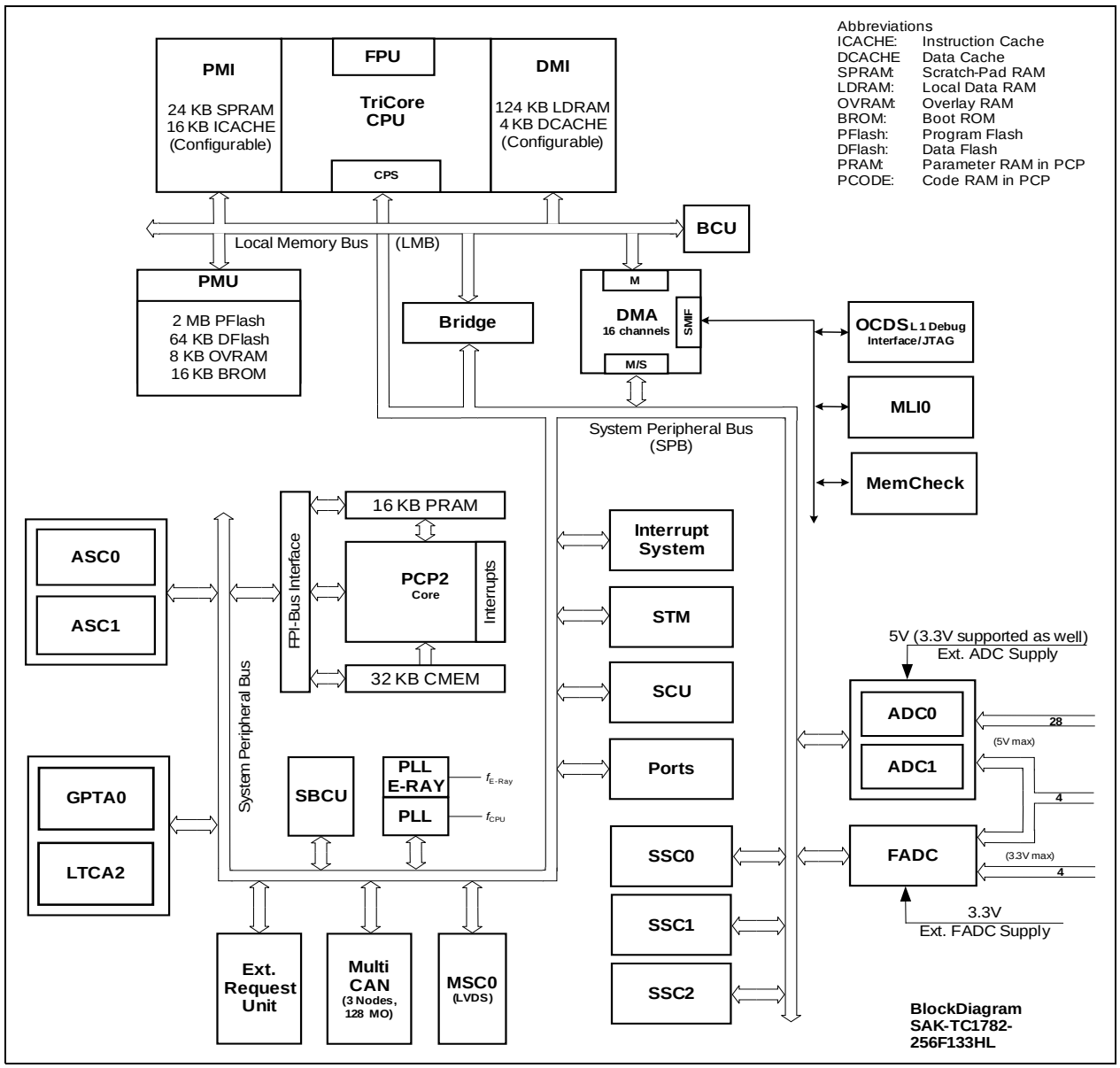


Figure 2 SAK-TC1782-256F133HL Block Diagram

1 Pinning

Figure 1 is showing the TC1782 Logic Symbol.

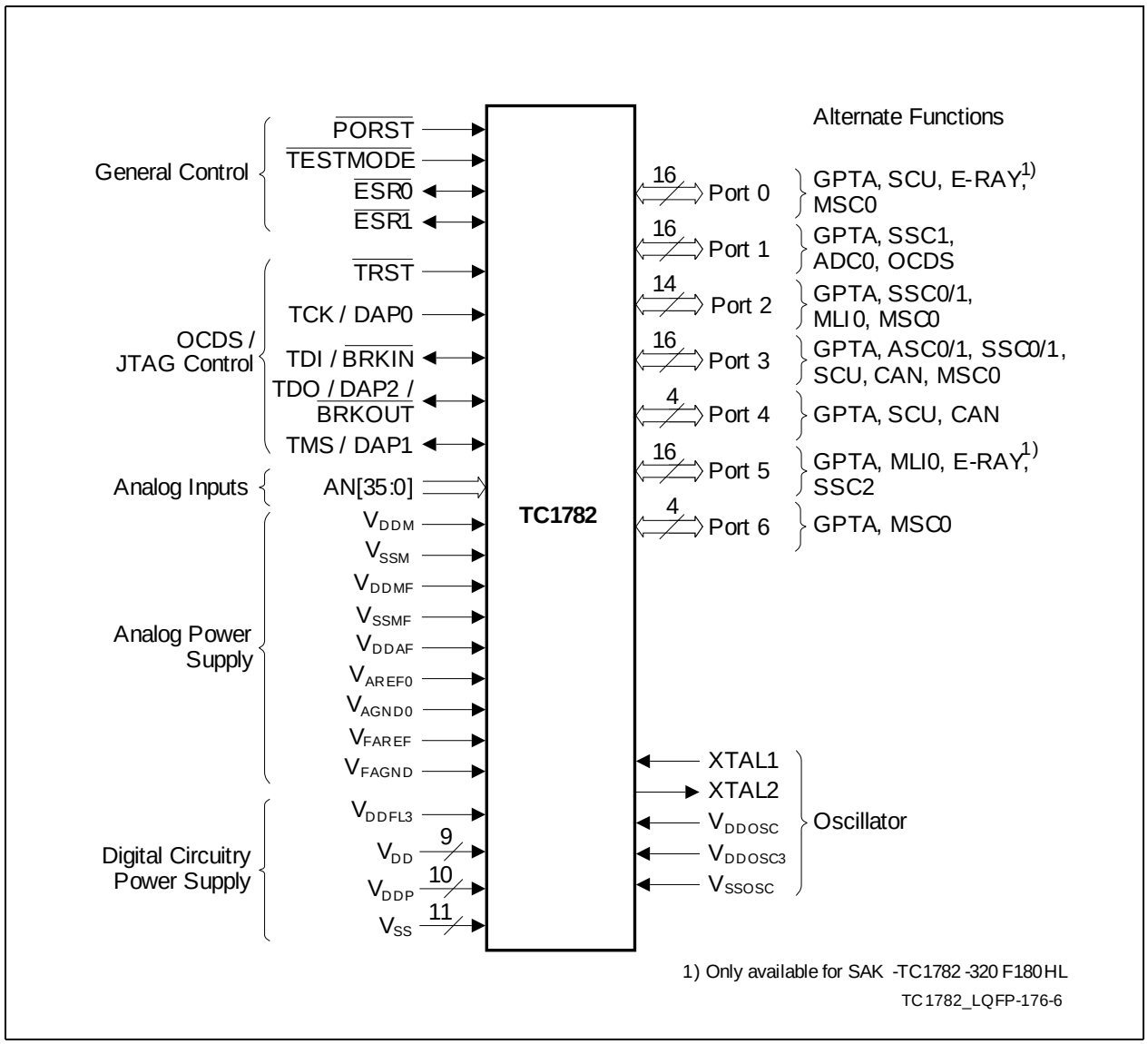


Figure 1 TC1782 Logic Symbol

1.1 TC1782 Pin Configuration

This chapter shows the pin configuration of the TC1782 package PG-LQFP-176-6.

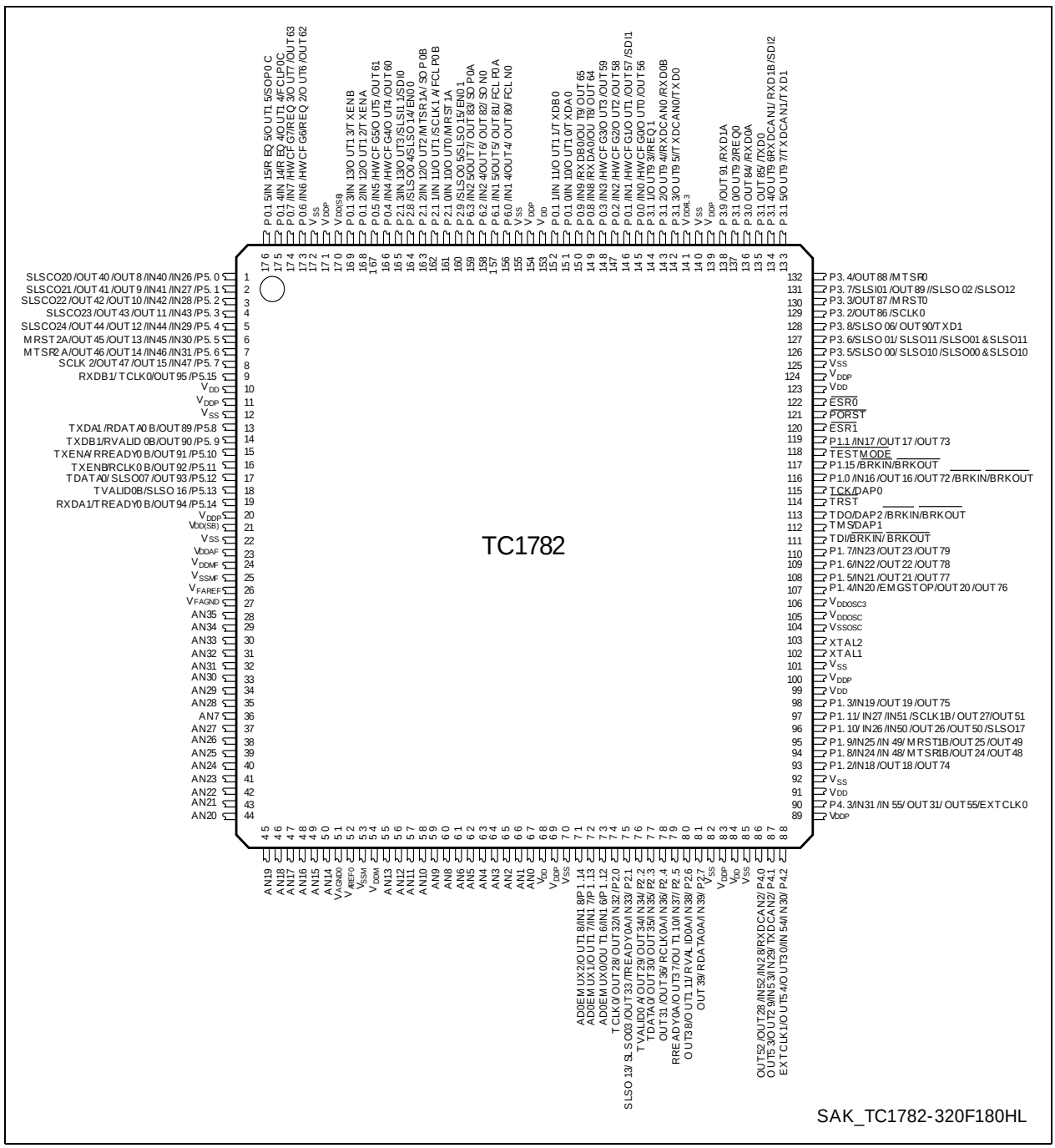


Figure 2 SAK-TC1782-320F180HL Pinning

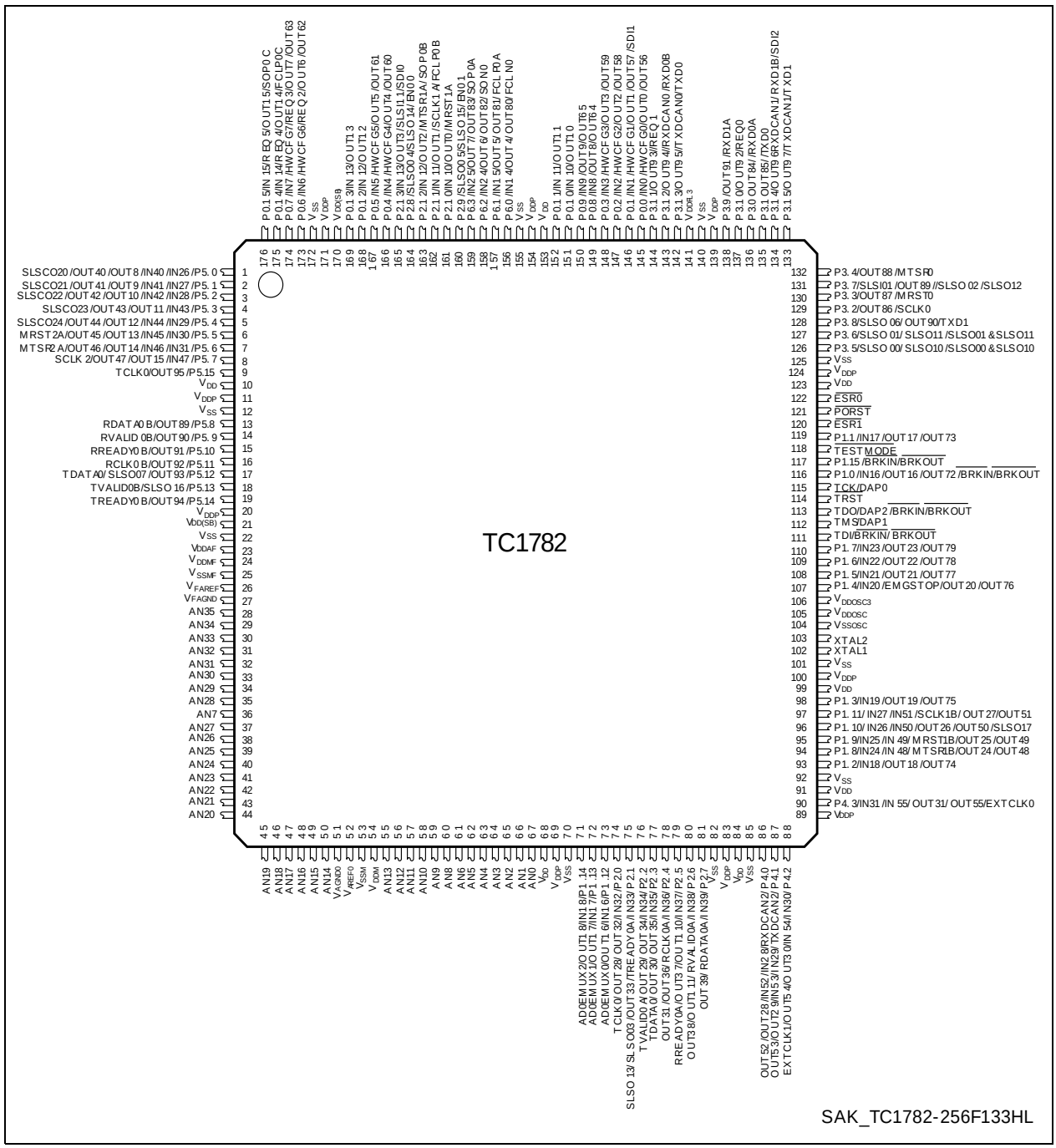


Figure 3 SAK-TC1782-256F133HL Pinning

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package)

Pin	Symbol	Ctrl.	Type	Function
Port 0				

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
145	P0.0	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 0**
	IN0	I		**GPTA0 Input 0**
	IN0	I		**LTCA2 Input 0**
	HWCFG0	I		**Hardware Configuration Input 0**
	OUT0	O1		**GPTA0 Output 0**
	OUT56	O2		**GPTA0 Output 56**
	OUT0	O3		**LTCA2 Output 0**
146	P0.1	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 1**
	IN1	I		**GPTA0 Input 1**
	IN1	I		**LTCA2 Input 1**
	SDI1	I		**MSC0 Serial Data Input 1**
	HWCFG1	I		**Hardware Configuration Input 1**
	OUT1	O1		**GPTA0 Output 1**
	OUT57	O2		**GPTA0 Output 57**
	OUT1	O3		**LTCA2 Output 1**
147	P0.2	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 2**
	IN2	I		**GPTA0 Input 2**
	IN2	I		**LTCA2 Input 2**
	HWCFG2	I		**Hardware Configuration Input 2**
	OUT2	O1		**GPTA0 Output 2**
	OUT58	O2		**GPTA0 Output 58**
	OUT2	O3		**LTCA2 Output 2**
148	P0.3	I/O0	A+1/ PU	**Port 0 General Purpose I/O Line 3**
	IN3	I		**GPTA0 Input 3**
	IN3	I		**LTCA2 Input 3**
	HWCFG3	I		**Hardware Configuration Input 3**
	OUT3	O1		**GPTA0 Output 3**
	OUT59	O2		**GPTA0 Output 59**
	OUT3	O3		**LTCA2 Output 3**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
166	P0.4	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 4**
	IN4	I		**GPTA0 Input 4**
	IN4	I		**LTCA2 Input 4**
	HWCFG4	I		**Hardware Configuration Input 4**
	OUT4	O1		**GPTA0 Output 4**
	OUT60	O2		**GPTA0 Output 60**
	OUT4	O3		**LTCA2 Output 4**
167	P0.5	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 5**
	IN5	I		**GPTA0 Input 5**
	IN5	I		**LTCA2 Input 5**
	HWCFG5	I		**Hardware Configuration Input 5**
	OUT5	O1		**GPTA0 Output 5**
	OUT61	O2		**GPTA0 Output 61**
	OUT5	O3		**LTCA2 Output 5**
173	P0.6	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 6**
	IN6	I		**GPTA0 Input 6**
	IN6	I		**LTCA2 Input 6**
	HWCFG6	I		**Hardware Configuration Input 6**
	REQ2	I		**External Request Input 2**
	OUT6	O1		**GPTA0 Output 6**
	OUT62	O2		**GPTA0 Output 62**
	OUT6	O3		**LTCA2 Output 6**
174	P0.7	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 7**
	IN7	I		**GPTA0 Input 7**
	IN7	I		**LTCA2 Input 7**
	HWCFG7	I		**Hardware Configuration Input 7**
	REQ3	I		**External Request Input 3**
	OUT7	O1		**GPTA0 Output 7**
	OUT63	O2		**GPTA0 Output 63**
	OUT7	O3		**LTCA2 Output 7**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
149	P0.8	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 8**
	IN8	I		**GPTA0 Input 8**
	IN8	I		**LTCA2 Input 8**
	RXDA0	I		**E-Ray Channel A Receive Data Input 0 [1)]**
	OUT8	O1		**GPTA0 Output 8**
	OUT64	O2		**GPTA0 Output 64**
	OUT8	O3		**LTCA2 Output 8**
150	P0.9	I/O0	A1/ PU	**Port 0 General Purpose I/O Line 9**
	IN9	I		**GPTA0 Input 9**
	IN9	I		**LTCA2 Input 9**
	RXDB0	I		**E-Ray Channel B Receive Data Input 0 [1)]**
	OUT9	O1		**GPTA0 Output 9**
	OUT65	O2		**GPTA0 Output 65**
	OUT9	O3		**LTCA2 Output 9**
151	P0.10	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 10**
	IN10	I		**GPTA0 Input 10**
	OUT10	O1		**GPTA0 Output 10**
	TXDA0	O2		**E-Ray Channel A transmit Data Output [1)]**
	OUT10	O3		**LTCA2 Output 10**
152	P0.11	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 11**
	IN11	I		**GPTA0 Input 11**
	OUT11	O1		**GPTA0 Output 11**
	TXDB0	O2		**E-Ray Channel B transmit Data Output [1)]**
	OUT11	O3		**LTCA2 Output 11**
168	P0.12	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 12**
	IN12	I		**GPTA0 Input 12**
	OUT12	O1		**GPTA0 Output 12**
	TXENA	O2		**E-Ray Channel A transmit Data Output enable [1)]**
	OUT12	O3		**LTCA2 Output 12**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
169	P0.13	I/O0	A2/ PU	**Port 0 General Purpose I/O Line 13**
	IN13	I		**GPTA0 Input 13**
	OUT13	O1		**GPTA0 Output 13**
	TXENB	O2		**E-Ray Channel B transmit Data Output enable** 1)
	OUT13	O3		**LTCA2 Output 13**
175	P0.14	I/O0	A1+/ PU	**Port 0 General Purpose I/O Line 14**
	IN14	I		**GPTA0 Input 14**
	REQ4	I		**External Request Input 4**
	OUT14	O1		**GPTA0 Output 14**
	FCLP0C	O2		**MSC0 Clock Output Positive C**
	OUT14	O3		**LTCA2 Output 14**
176	P0.15	I/O0	A1+/ PU	**Port 0 General Purpose I/O Line 15**
	IN15	I		**GPTA0 Input 15**
	REQ5	I		**External Request Input 5**
	OUT15	O1		**GPTA0 Output 15**
	SOP0C	O2		**MSC0 Serial Data Output Positive C**
	OUT15	O3		**LTCA2 Output 15**
Port 1				
116	P1.0	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 0**
	IN16	I		**GPTA0 Input 16**
	$\overline{\text{BRKIN}}$	I		**Break Input**
	OUT16	O1		**GPTA0 Output 16**
	OUT72	O2		**GPTA0 Output 72**
	OUT16	O3		**LTCA2 Output 16**
	$\overline{\text{BRKOUT}}$	O		**Break Output (controlled by OCDS module)**
119	P1.1	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 1**
	IN17	I		**GPTA0 Input 17**
	OUT17	O1		**GPTA0 Output 17**
	OUT73	O2		**GPTA0 Output 73**
	OUT17	O3		**LTCA2 Output 17**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
93	P1.2	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 2**
	IN18	I		**GPTA0 Input 18**
	OUT18	O1		**GPTA0 Output 18**
	OUT74	O2		**GPTA0 Output 74**
	OUT18	O3		**LTCA2 Output 18**
98	P1.3	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 3**
	IN19	I		**GPTA0 Input 19**
	IN19	I		**LTCA2 Input 19**
	OUT19	O1		**GPTA0 Output 19**
	OUT75	O2		**GPTA0 Output 75**
	OUT19	O3		**LTCA2 Output 19**
107	P1.4	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 4**
	IN20	I		**GPTA0 Input 20**
	IN20	I		**LTCA2 Input 20**
	EMGSTOP	I		**Emergency Stop Input**
	OUT20	O1		**GPTA0 Output 20**
	OUT76	O2		**GPTA0 Output 76**
	OUT20	O3		**LTCA2 Output 20**
108	P1.5	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 35**
	IN21	I		**GPTA0 Input 21**
	IN21	I		**LTCA2 Input 21**
	OUT21	O1		**GPTA0 Output 21**
	OUT77	O2		**GPTA0 Output 77**
	OUT21	O3		**LTCA2 Output 21**
109	P1.6	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 6**
	IN22	I		**GPTA0 Input 22**
	IN22	I		**LTCA2 Input 22**
	OUT22	O1		**GPTA0 Output 22**
	OUT78	O2		**GPTA0 Output 78**
	OUT22	O3		**LTCA2 Output 22**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
110	P1.7	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 7**
	IN23	I		**GPTA0 Input 23**
	IN23	I		**LTCA2 Input 23**
	OUT23	O1		**GPTA0 Output 23**
	OUT79	O2		**GPTA0 Output 79**
	OUT23	O3		**LTCA2 Output 23**
94	P1.8	I/O0	A1+/ PU	**Port 1 General Purpose I/O Line 8**
	IN24	I		**GPTA0 Input 24**
	IN48	I		**GPTA0 Input 48**
	MTSR1B	I		**SSC1 Slave Receive Input B (Slave Mode)**
	OUT24	O1		**GPTA0 Output 24**
	OUT48	O2		**GPTA0 Output 48**
	MTSR1B	O3		**SSC1 Master Transmit Output B (Master Mode)**
95	P1.9	I/O0	A1+/ PU	**Port 1 General Purpose I/O Line 9**
	IN25	I		**GPTA0 Input 25**
	IN49	I		**GPTA0 Input 49**
	MRST1B	I		**SSC1 Master Receive Input B (Master Mode)**
	OUT25	O1		**GPTA0 Output 25**
	OUT49	O2		**GPTA0 Output 49**
	MRST1B	O3		**SSC1 Slave Transmit Output B (Slave Mode)**
96	P1.10	I/O0	A1+/ PU	**Port 1 General Purpose I/O Line 10**
	IN26	I		**GPTA0 Input 26**
	IN50	I		**GPTA0 Input 50**
	OUT26	O1		**GPTA0 Output 26**
	OUT50	O2		**GPTA0 Output 50**
	SLSO17	O3		**SSC1 Slave Select Output 7**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	P1.11	I/O0	A1+/ PU	**Port 1 General Purpose I/O Line 11**
	IN27	I		**GPTA0 Input 27**
	IN51	I		**GPTA0 Input 51**
	SCLK1B	I		**SSC1 Clock Input B**
	OUT27	O1		**GPTA0 Output 27**
	OUT51	O2		**GPTA0 Output 51**
	SCLK1B	O3		**SSC1 Clock Output B**
73	P1.12	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 12**
	IN16	I		**LTCA2 Input 16**
	AD0EMUX0	O1		**ADC0 External Multiplexer Control Output 0**
	AD0EMUX0	O2		**ADC0 External Multiplexer Control Output 0**
	OUT16	O3		**LTCA2 Output 16**
72	P1.13	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 13**
	IN17	I		**LTCA2 Input 17**
	AD0EMUX1	O1		**ADC0 External Multiplexer Control Output 1**
	AD0EMUX1	O2		**ADC0 External Multiplexer Control Output 1**
	OUT17	O3		**LTCA2 Output 17**
71	P1.14	I/O0	A1/ PU	**Port 1 General Purpose I/O Line 14**
	IN18	I		**LTCA2 Input 18**
	AD0EMUX2	O1		**ADC0 External Multiplexer Control Output 2**
	AD0EMUX2	O2		**ADC0 External Multiplexer Control Output 2**
	OUT18	O3		**LTCA2 Output 18**
117	P1.15	I/O0	A2/ PU	**Port 1 General Purpose I/O Line 15**
	$\overline{\text{BRKIN}}$	I		**Break Input**
	Reserved	O1		**-**
	Reserved	O2		**-**
	Reserved	O3		**-**
	$\overline{\text{BRKOUT}}$	O		**Break Output (controlled by OCDS module)**

Port 2

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
74	P2.0	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 0**
	IN32	I		**GPTA0 Input 32**
	OUT32	O1		**GPTA0 Output 32**
	TCLK0	O2		**MLI0 Transmitter Clock Output 0**
	OUT28	O3		**LTCA2 Output 28**
75	P2.1	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 1**
	IN33	I		**GPTA0 Input 33**
	TREADY0A	I		**MLI0 Transmitter Ready Input A**
	OUT33	O1		**GPTA0 Output 33**
	SLSO03	O2		**SSC0 Slave Select Output Line 3**
	SLSO13	O3		**SSC1 Slave Select Output Line 3**
76	P2.2	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 2**
	IN34	I		**GPTA0 Input 34**
	OUT34	O1		**GPTA0 Output 34**
	TVALID0	O2		**MLI0 Transmitter Valid Output**
	OUT29	O3		**LTCA2 Output 29**
77	P2.3	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 3**
	IN35	I		**GPTA0 Input 35**
	OUT35	O1		**GPTA0 Output 35**
	TDATA0	O2		**MLI0 Transmitter Data Output**
	OUT30	O3		**LTCA2 Output 30**
78	P2.4	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 4**
	IN36	I		**GPTA0 Input 36**
	RCLK0A	I		**MLI Receiver Clock Input A**
	OUT36	O1		**GPTA0 Output 36**
	OUT36	O2		**GPTA0 Output 36**
	OUT31	O3		**LTCA2 Output 31**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
79	P2.5	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 5**
	IN37	I		**GPTA0 Input 37**
	OUT37	O1		**GPTA0 Output 37**
	RREADY0A	O2		**MLI0 Receiver Ready Output A**
	OUT110	O3		**LTCA2 Output 110**
80	P2.6	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 6**
	IN38	I		**GPTA0 Input 38**
	RVALID0A	I		**MLI Receiver Valid Input A**
	OUT38	O1		**GPTA0 Output 38**
	OUT38	O2		**GPTA0 Output 38**
	OUT111	O3		**LTCA2 Output 111**
81	P2.7	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 7**
	IN39	I		**GPTA0 Input 39**
	RDATA0A	I		**MLI Receiver Data Input A**
	OUT39	O1		**GPTA0 Output 39**
	OUT39	O2		**GPTA0 Output 39**
	Reserved	O3		**-**
164	P2.8	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 8**
	SLSO04	O1		**SSC0 Slave Select Output 4**
	SLSO14	O2		**SSC1 Slave Select Output 4**
	EN00	O3		**MSC0 Enable Output 0**
160	P2.9	I/O0	A2/ PU	**Port 2 General Purpose I/O Line 9**
	SLSO05	O1		**SSC0 Slave Select Output 5**
	SLSO15	O2		**SSC1 Slave Select Output 5**
	EN01	O3		**MSC0 Enable Output 1**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
161	P2.10	I/O0	A1+/ PU	**Port 2 General Purpose I/O Line 10**
	MRST1A	I		**SSC1 Master Receive Input A**
	IN10	I		**LTCA2 Input 10**
	MRST1A	O1		**SSC1 Slave Transmit Output**
	OUT0	O2		**LTCA2 Output 0**
	Reserved	O3		**-**
162	P2.11	I/O0	A1+/ PU	**Port 2 General Purpose I/O Line 11**
	SCLK1A	I		**SSC1 Clock Input A**
	IN11	I		**LTCA2 Input 11**
	SCLK1A	O1		**SSC1 Clock Output A**
	OUT1	O2		**LTCA2 Output 1**
	FCLP0B	O3		**MSC0 Clock Output Positive B**
163	P2.12	I/O0	A1+/ PU	**Port 2 General Purpose I/O Line 12**
	MTSR1A	I		**SSC1 Slave Receive Input A**
	IN12	I		**LTCA2 Input 12**
	MTSR1A	O1		**SSC1 Master Transmit Output A**
	OUT2	O2		**LTCA2 Output 2**
	SOP0B	O3		**MSC0 Serial Data Output Positive B**
165	P2.13	I/O0	A1/ PU	**Port 2 General Purpose I/O Line 13**
	SLSI11	I		**SSC1 Slave Select Input 1**
	SDI0	I		**MSC0 Serial Data Input 0**
	IN13	I		**LTCA2 Input 13**
	OUT3	O1		**LTCA2 Output 3**
	Reserved	O2		**-**
	Reserved	O3		**-**
Port 3				

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
136	P3.0	I/O0	A1+/ PU	**Port 3 General Purpose I/O Line 0**
	RXD0A	I		**ASC0 Receiver Input A (Async. & Sync. Mode)**
	RXD0A	O1		**ASC0 Output (Sync. Mode)**
	RXD0A	O2		**ASC0 Output (Sync. Mode)**
	OUT84	O3		**GPTA0 Output 84**
135	P3.1	I/O0	A1+/ PU	**Port 3 General Purpose I/O Line 1**
	TXD0	O1		**ASC0 Output**
	TXD0	O2		**ASC0 Output**
	OUT85	O3		**GPTA0 Output 85**
129	P3.2	I/O0	A1+/ PU	**Port 3 General Purpose I/O Line 2**
	SCLK0	I		**SSC0 Clock Input (Slave Mode)**
	SCLK0	O1		**SSC0 Clock Output (Master Mode)**
	SCLK0	O2		**SSC0 Clock Output (Master Mode)**
	OUT86	O3		**GPTA0 Output 86**
130	P3.3	I/O0	A1+/ PU	**Port 3 General Purpose I/O Line 3**
	MRST0	I		**SSC0 Master Receive Input (Master Mode)**
	MRST0	O1		**SSC0 Slave Transmit Output (Slave Mode)**
	MRST0	O2		**SSC0 Slave Transmit Output (Slave Mode)**
	OUT87	O3		**GPTA0 Output 87**
132	P3.4	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 4**
	MTSR0	I		**SSC0 Slave Receive Input (Slave Mode)**
	MTSR0	O1		**SSC0 Master Transmit Output (Master Mode)**
	MTSR0	O2		**SSC0 Master Transmit Output (Master Mode)**
	OUT88	O3		**GPTA0 Output 88**
126	P3.5	I/O0	A1+/ PU	**Port 3 General Purpose I/O Line 5**
	SLSO00	O1		**SSC0 Slave Select Output 0**
	SLSO10	O2		**SSC1 Slave Select Output 0**
	SLSOANDO0	O3		**SSC0 AND SSC1 Slave Select Output 0**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
127	P3.6	I/O0	A1+/ PU	**Port 3 General Purpose I/O Line 6**
	SLSO01	O1		**SSC0 Slave Select Output 1**
	SLSO11	O2		**SSC1 Slave Select Output 1**
	SLSOANDO1	O3		**SSC0 AND SSC1 Slave Select Output 1**
131	P3.7	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 7**
	SLSI01	I		**SSC0 Slave Select Input 1**
	SLSO02	O1		**SSC0 Slave Select Output 2**
	SLSO12	O2		**SSC1 Slave Select Output 2**
	OUT89	O3		**GPTA0 Output 89**
128	P3.8	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 8**
	SLSO06	O1		**SSC0 Slave Select Output 6**
	TXD1	O2		**ASC1 Transmit Output**
	OUT90	O3		**GPTA0 Output 90**
138	P3.9	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 9**
	RXD1A	I		**ASC1 Receiver Input A**
	RXD1A	O1		**ASC1 Receiver Output A (Synchronous Mode)**
	RXD1A	O2		**ASC1 Receiver Output A (Synchronous Mode)**
	OUT91	O3		**GPTA0 Output 91**
137	P3.10	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 10**
	REQ0	I		**External Request Input 0**
	Reserved	O1		**-**
	Reserved	O2		**-**
	OUT92	O3		**GPTA0 Output 92**
144	P3.11	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 11**
	REQ1	I		**External Request Input 1**
	Reserved	O1		**-**
	Reserved	O2		**-**
	OUT93	O3		**GPTA0 Output 93**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
143	P3.12	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 12**
	RXDCAN0	I		**CAN Node 0 Receiver Input**
	RXD0B	I		**ASC0 Receiver Input B**
	RXD0B	O1		**ASC0 Receiver Output B (Synchronous Mode)**
	RXD0B	O2		**ASC0 Receiver Output B (Synchronous Mode)**
	OUT94	O3		**GPTA0 Output 94**
142	P3.13	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 13**
	TXDCAN0	O1		**CAN Node 0 Transmitter Output**
	TXD0	O2		**ASC0 Transmit Output**
	OUT95	O3		**GPTA0 Output 95**
134	P3.14	I/O0	A1/ PU	**Port 3 General Purpose I/O Line 14**
	RXDCAN1	I		**CAN Node 1 Receiver Input**
	RXD1B	I		**ASC1 Receiver Input B**
	SDI2	I		**MSC0 Serial Data Input 2**
	RXD1B	O1		**ASC1 Receiver Output B (Synchronous Mode)**
	RXD1B	O2		**ASC1 Receiver Output B (Synchronous Mode)**
	OUT96	O3		**GPTA0 Output 96**
133	P3.15	I/O0	A2/ PU	**Port 3 General Purpose I/O Line 15**
	TXDCAN1	O1		**CAN Node 1 Transmitter Output**
	TXD1	O2		**ASC1 Transmit Output**
	OUT97	O3		**GPTA0 Output 97**
Port 4				
86	P4.0	I/O0	A1+/ PU	**Port 4 General Purpose I/O Line 0**
	IN28	I		**GPTA0 Input 28**
	IN52	I		**GPTA0 Input 52**
	RXDCAN2	I		**CAN Node 2 Receiver Input**
	OUT28	O1		**GPTA0 Output 28**
	OUT52	O2		**GPTA0 Output 52**
	Reserved	O3		**-**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
87	P4.1	I/O0	A1+/ PU	**Port 4 General Purpose I/O Line 1**
	IN29	I		**GPTA0 Input 29**
	IN53	I		**GPTA0 Input 53**
	OUT29	O1		**GPTA0 Output 29**
	OUT53	O2		**GPTA0 Output 53**
	TXDCAN2	O3		**CAN Node 2 Transmitter Output**
88	P4.2	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 2**
	IN30	I		**GPTA0 Input 30**
	IN54	I		**GPTA0 Input 54**
	OUT30	O1		**GPTA0 Output 30**
	OUT54	O2		**GPTA0 Output 54**
	EXTCLK1	O3		**External Clock 1 Output**
90	P4.3	I/O0	A2/ PU	**Port 4 General Purpose I/O Line 3**
	IN31	I		**GPTA0 Input 31**
	IN55	I		**GPTA0 Input 55**
	OUT31	O1		**GPTA0 Output 31**
	OUT55	O2		**GPTA0 Output 55**
	EXTCLK0	O3		**External Clock 0 Output**
Port 5				
1	P5.0	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 0**
	IN40	I		**GPTA0 Input 40**
	IN26	I		**LTCA2 Input 26**
	OUT40	O1		**GPTA0 Output 40**
	OUT8	O2		**LTCA2 Output 8**
	SLSO20	O3		**SSC2 Slave Select Output 0**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2	P5.1	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 1**
	IN41	I		**GPTA0 Input 41**
	IN27	I		**LTCA2 Input 27**
	OUT41	O1		**GPTA0 Output 41**
	OUT9	O2		**LTCA2 Output 9**
	SLSO21	O3		**SSC2 Slave Select Output 1**
3	P5.2	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 2**
	IN42	I		**GPTA0 Input 42**
	IN28	I		**LTCA2 Input 28**
	OUT42	O1		**GPTA0 Output 42**
	OUT10	O2		**LTCA2 Output 10**
	SLSO22	O3		**SSC2 Slave Select Output 2**
4	P5.3	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 3**
	IN43	I		**GPTA0 Input 43**
	OUT43	O1		**GPTA0 Output 43**
	OUT11	O2		**LTCA2 Output 11**
	SLSO23	O3		**SSC2 Slave Select Output 3**
5	P5.4	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 4**
	IN44	I		**GPTA0 Input 44**
	IN29	I		**LTCA2 Input 29**
	SLSI2A	I		**SSC2 Slave Select Input A**
	OUT44	O1		**GPTA0 Output 44**
	OUT12	O2		**LTCA2 Output 12**
	SLSO24	O3		**SSC2 Slave Select Output 4**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P5.5	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 5**
	IN45	I		**GPTA0 Input 45**
	IN30	I		**LTCA2 Input 30**
	MRST2A	I		**SSC2 Master Receive Input (Master Mode)**
	OUT45	O1		**GPTA0 Output 45**
	OUT13	O2		**LTCA2 Output 13**
	MRST2	O3		**SSC2 Master Transmit Input (Slave Mode)**
7	P5.6	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 6**
	IN46	I		**GPTA0 Input 46**
	IN31	I		**LTCA2 Input 31**
	MTSR2A	I		**SSC2 Slave Receive Input (Slave Mode)**
	OUT46	O1		**GPTA0 Output 46**
	OUT14	O2		**LTCA2 Output 14**
	MTSR2	O3		**SSC2 Master Transmit Output (Master Mode)**
8	P5.7	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 7**
	IN47	I		**GPTA0 Input 47**
	SCLK2A	I		**SSC2 Clock Input (Slave Mode)**
	OUT47	O1		**GPTA0 Output 47**
	OUT15	O2		**LTCA2 Output 15**
	SCLK2	O3		**SSC2 Clock Output (Master Mode)**
13	P5.8	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 8**
	RDATA0B	I		**MLI0 Receiver Data Input B**
	Reserved	O1		**-**
	TXDA1	O2		**E-Ray Channel A transmit Data Output** [1]
	OUT89	O3		**LTCA2 Output 89**
14	P5.9	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 9**
	RVALID0B	I		**MLI0 Receiver Data Valid Input B**
	Reserved	O1		**-**
	TXDB1	O2		**E-Ray Channel B transmit Data Output** [1]
	OUT90	O3		**LTCA2 Output 90**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
15	P5.10	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 10**
	RREADY0B	O1		**MLI0 Receiver Ready Input B**
	TXENA	O2		**E-Ray Channel A transmit Data Output enable** 1)
	OUT91	O3		**LTCA2 Output 91**
16	P5.11	I/O0	A2/ PU	**Port 5 General Purpose I/O Line 11**
	RCLK0B	I		**MLI0 Receiver Clock Input B**
	Reserved	O1		**-**
	TXENB	O2		**E-Ray Channel B transmit Data Output enable** 1)
	OUT92	O3		**LTCA2 Output 92**
17	P5.12	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 12**
	TDATA0	O1		**MLI0 Transmitter Data Output**
	SLSO07	O2		**SSC0 Slave Select Output 7**
	OUT93	O3		**LTCA2 Output 93**
18	P5.13	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 13**
	TVALID0B	O1		**MLI0 Transmitter Valid Input B**
	SLSO16	O2		**SSC1 Slave Select Output 6**
	Reserved	O3		**-**
19	P5.14	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 14**
	TREADY0B	I		**MLI0 Transmitter Ready Input B**
	RXDA1	I		**E-Ray Channel A Receive Data Input 1** 1)
	Reserved	O1		**-**
	Reserved	O2		**-**
	OUT94	O3		**LTCA2 Output 94**
9	P5.15	I/O0	A1+/ PU	**Port 5 General Purpose I/O Line 15**
	RXDB1	I		**E-Ray Channel B Receive Data Input 1** 1)
	TCLK0	O1		**MLI0 Transmitter Clock Output**
	Reserved	O2		**-**
	OUT95	O3		**LTCA2 Output 95**
Port 6				

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
156	P6.0	I/O0	A1/ F/ PU	**Port 6 General Purpose I/O Line 0**
	IN14	I		**LTCA2 Input 14**
	FCLN0	O1		**MSC0 Clock Output Negative**
	OUT80	O2		**GPTA0 Output 80**
	OUT4	O3		**LTCA2 Output 4**
157	P6.1	I/O0	A1/ F/ PU	**Port 6 General Purpose I/O Line 1**
	IN15	I		**LTCA2 Input 15**
	FCLP0A	O1		**MSC0 Clock Output Positive A**
	OUT81	O2		**GPTA0 Output 81**
	OUT5	O3		**LTCA2 Output 5**
158	P6.2	I/O0	A1/ F/ PU	**Port 6 General Purpose I/O Line 2**
	IN24	I		**LTCA2 Input 24**
	SON0	O1		**MSC0 Serial Data Output Negative**
	OUT82	O2		**GPTA0 Output 82**
	OUT6	O3		**LTCA2 Output 6**
159	P6.3	I/O0	A1/ F/ PU	**Port 6 General Purpose I/O Line 3**
	IN25	I		**LTCA2 Input 25**
	SOP0A	O1		**MSC0 Serial Data Output Positive A**
	OUT83	O2		**GPTA0 Output 83**
	OUT7	O3		**LTCA2 Output 7**
Analog Input Port				
67	AN0	I	D	**Analog Input 0**
66	AN1	I	D	**Analog Input 1**
65	AN2	I	D	**Analog Input 2**
64	AN3	I	D	**Analog Input 3**
63	AN4	I	D	**Analog Input 4**
62	AN5	I	D	**Analog Input 5**
61	AN6	I	D	**Analog Input 6**
36	AN7	I	D	**Analog Input 7**
60	AN8	I	D	**Analog Input 8**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
59	AN9	I	D	**Analog Input 9**
58	AN10	I	D	**Analog Input 10**
57	AN11	I	D	**Analog Input 11**
56	AN12	I	D	**Analog Input 12**
55	AN13	I	D	**Analog Input 13**
50	AN14	I	D	**Analog Input 14**
49	AN15	I	D	**Analog Input 15**
48	AN16	I	D	**Analog Input 16**
47	AN17	I	D	**Analog Input 17**
46	AN18	I	D	**Analog Input 18**
45	AN19	I	D	**Analog Input 19**
44	AN20	I	D	**Analog Input 20**
43	AN21	I	D	**Analog Input 21**
42	AN22	I	D	**Analog Input 22**
41	AN23	I	D	**Analog Input 23**
40	AN24	I	D	**Analog Input 24**
39	AN25	I	D	**Analog Input 25**
38	AN26	I	D	**Analog Input 26**
37	AN27	I	D	**Analog Input 27**
35	AN28	I	D	**Analog Input 28**
34	AN29	I	D	**Analog Input 29**
33	AN30	I	D	**Analog Input 30**
32	AN31	I	D	**Analog Input 31**
31	AN32	I	D	**Analog Input 32**
30	AN33	I	D	**Analog Input 33**
29	AN34	I	D	**Analog Input 34**
28	AN35	I	D	**Analog Input 35**
54	V_{DDM}	-	-	**ADC Analog Part Power Supply (3.3V - 5V)**
53	V_{SSM}	-	-	**ADC Analog Part Ground**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
52	V_{AREF0}	-	-	**ADC0 Reference Voltage**
	V_{AREF1}	-	-	**ADC1 Reference Voltage**
51	V_{AGND0}	-	-	**ADC Reference Ground**
24	V_{DDMF}	-	-	**FADC Analog Part Power Supply (3.3V)**
23	V_{DDAF}	-	-	**FADC Analog Part Logic Power Supply (1.3V)**
25	V_{SSMF}	-	-	**FADC Analog Part Ground**
	V_{SSAF}	-	-	**FADC Analog Part Ground**
26	V_{FAREF}	-	-	**FADC Reference Voltage**
27	V_{FAGND}	-	-	**FADC Reference Ground**
10, 21[2)], 68, 84, 91, 99, 123, 153, 170 [2)]	V_{DD}	-	-	**Digital Core Power Supply (1.3V)**
11, 20, 69, 83, 89, 100, 124, 139, 154, 171	V_{DDP}	-	-	**Port Power Supply (3.3V)**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
12, 22, 70, 82, 85, 92, 101, 125, 140, 155, 172	V_{SS}	-	-	**Digital Ground**
105	V_{DDOSC}	-	-	**Main Oscillator and PLL Power Supply (1.3V)**
106	V_{DDOSC3}	-	-	**Main Oscillator Power Supply (3.3V)**
104	V_{SSOSC}	-	-	**Main Oscillator and PLL Ground**
141	V_{DDFL3}	-	-	**Power Supply for Flash (3.3V)**
102	XTAL1	I		**Main Oscillator Input**
103	XTAL2	O		**Main Oscillator Output**
111	TDI	I	A2/ PU	**JTAG Serial Data Input**
	BRKIN	I		**OCDS Break Input Line**
	BRKOUT	O		**OCDS Break Output Line**
112	TMS	I	A2/ PD	**JTAG State Machine Control Input**
	DAP1	I/O		**Device Access Port Line 1**
113	TDO	I/O	A2/ PU	**JTAG Serial Data Output**
	DAP2	I/O		**Device Access Port Line 2**
	BRKIN	I		**OCDS Break Input Line**
	BRKOUT	O		**OCDS Break Output Line**
114	TRST	I	I / PD	**JTAG Reset Input**
115	TCK	I	A1/ PD	**JTAG Clock Input**
	DAP0	I		**Device Access Port Line 0**
118	TESTMODE	I	I / PU	**Test Mode Select Input**
120	ESR1	I/O	A2/ PD	**External System Request Reset Input 1**

Table 1 Pin Definitions and Functions (PG-LQFP-176-6 Package) (cont'd)

Pin	Symbol	Ctrl.	Type	Function
121	PORST	I	I / PD	**Power On Reset Input**
122	ESR0	I/O	A2	**External System Request Reset Input 0** Default configuration during and after reset is open-drain driver. The driver drives low during power-on reset.

1) Only available for SAK-TC1782-320F180HL.

2) For the emulation device (ED), this pin is bonded to VDDSB (ED Stand By RAM supply). In the production devide device, this pin is bonded to a VDD pad.

Legend for Table 1

Column "**Ctrl.**":

I = Input (for GPIO port lines with IOCR bit field selection PCx = $0XXX_B$)

O = Output
O0 = Output with IOCR bit field selection PCx = $1X00_B$
O1 = Output with IOCR bit field selection PCx = $1X01_B$ (ALT1)
O2 = Output with IOCR bit field selection PCx = $1X10_B$(ALT2)
O3 = Output with IOCR bit field selection PCx = 1X11(ALT3)

Column "**Type**":

A1 = Pad class A1 (LVTTL)
A2 = Pad class A2 (LVTTL)
A5 = Pad class A5 (LVTTL)
F = Pad class F (LVDS/CMOS)
D = Pad class D (ADC)

PU = with pull-up device connected during reset ($\overline{\text{PORST}}$ = 0)
PD = with pull-down device connected during reset ($\overline{\text{PORST}}$ = 0)
TR = tri-state during reset ($\overline{\text{PORST}}$ = 0)

1 Identification Registers

The Identification Registers uniquely identify the whole device.

Table 1 SAK-TC1782-320F180HL Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	$0000\ 6350_H$	$F000\ 0408_H$	AB
CBS_JTAGID	$1018\ E083_H$	$F000\ 0464_H$	AB
SCU_CHIPID	$0500\ 9301_H$	$F000\ 0640_H$	AB
SCU_MANID	$0000\ 1820_H$	$F000\ 0644_H$	AB
SCU_RTID	$0000\ 0002_H$	$F000\ 0648_H$	AB

Table 2 SAK-TC1782-256F133HL Identification Registers

Short Name	Value	Address	Stepping
CBS_JDPID	$0000\ 6350_H$	$F000\ 0408_H$	AB
CBS_JTAGID	$1018\ E083_H$	$F000\ 0464_H$	AB
SCU_CHIPID	$1400\ 9301_H$	$F000\ 0640_H$	AB
SCU_MANID	$0000\ 1820_H$	$F000\ 0644_H$	AB
SCU_RTID	$0000\ 0002_H$	$F000\ 0648_H$	AB

1 Electrical Parameters

This specification provides all electrical parameters of the TC1782.

1.1 General Parameters

1.1.1 Parameter Interpretation

The parameters listed in this section partly represent the characteristics of the TC1782 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are marked with an two-letter abbreviation in column “Symbol”:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics which are a distinctive feature of the TC1782 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements which must provided by the microcontroller system in which the TC1782 designed in.

1.1.2 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and its basic characteristics. More details (mainly DC parameters) are defined in the **Section 1.2.1**.

Table 1 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub Class	Speed Grade	Load	Leakage 150°C	Termination
A	3.3 V	LVTTL I/O, LVTTL outputs	**A1** (e.g. GPIO)	6 MHz	100 pF	500 nA	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	1 µA	Series termination recommended
			A2 (e.g. serial I/Os)	40 MHz	50 pF	3 µA	Series termination recommended
F	3.3 V	LVDS	–	50 MHz	–	–	Parallel termination, 100 Ω ± 10% 1)
		CMOS	–	6 MHz	50 pF	–	
D_E	5 V	ADC	–	–	–	–	
I	3.3 V	LVTTL (input only)	–	–	–	–	

1) In applications where the LVDS pins are not used (disabled), these pins must be either left unconnected, or properly terminated with the differential parallel termination of 100 Ω ± 10%.

1.1.3 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Voltage at 1.3 V power supply pins with respect to V_{SS}	V_{DD}	SR	–	–	2.0	V	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage at 5 V power supply pins with respect to V_{SS}	V_{DDM}	SR	–	–	7.0	V	–
Voltage on any Class A input pin and dedicated input pins with respect to V_{SS}	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 4.3	V	Whatever is lower
Voltage on any Class D analog input pin with respect to V_{AGND}	V_{AIN} V_{AREFx}	SR	-0.5	–	7.0	V	–
Voltage on any shared Class D analog input pin with respect to V_{SSAF}, if the FADC is switched through to the pin.	V_{AINF} V_{FAREF}	SR	-0.5	–	7.0	V	–

1.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the TC1782. All parameters specified in the following tables refer to these operating conditions, unless otherwise noticed.

Digital supply voltages applied to the TC1782 must be static regulated voltages which allow a typical voltage swing of ± 5 %.

Table 3 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Overload coupling factor for analog inputs, negative	K_{OVAN} CC	–	–	0.0005		I_{OV}≤ 0 mA; I_{OV}≥ -1 mA; analog pad= 5.0 V
Overload coupling factor for analog inputs, positive	K_{OVAP} CC	–	–	0.00005		I_{OV}≤ 3 mA; I_{OV}≥ 0 mA; analog pad= 5.0 V
CPU Frequency	f_{CPU} SR	–	–	133	MHz	*product*= SAK-TC1782-256F 133HL
		–	–	180	MHz	*product*= SAK-TC1782-320F 180HL
FPI bus frequency	f_{FPI} SR	–	–	90	MHz	
LMB frequency	f_{LMB} CC	–	–	133	MHz	*product*= SAK-TC1782-256F 133HL
		–	–	180	MHz	*product*= SAK-TC1782-320F 180HL
PCP Frequency	f_{PCP} SR	–	–	133	MHz	*product*= SAK-TC1782-256F 133HL
		–	–	180	MHz	*product*= SAK-TC1782-320F 180HL

Table 3 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Inactive device pin current	I_{ID} SR	-1	–	1	mA	*All power supply voltages* V_{DDx} = 0
Short circuit current of digital outputs[1]	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device[2]	ΣI_{SC_D} CC	–	–	100	mA	
Absolute sum of short circuit currents per pin group[2]	ΣI_{SC_PG} CC	–	–	20	mA	
Ambient Temperature	T_A SR	-40	–	125	°C	
Junction temperature	T_J SR	-40	–	150	°C	
Core Supply Voltage	V_{DD} SR	1.235	1.3	1.365[3]	V	
Flash supply voltage 3.3V	V_{DDFL3} SR	3.13	3.3	3.47[4]	V	
ADC analog supply voltage	V_{DDM} SR	3.13	3.3	5.5	V	
Oscillator core supply voltage	V_{DDOSC} SR	1.235	1.3	1.365[3]	V	
Oscillator 3.3V supply voltage	V_{DDOSC3} SR	3.13	3.3	3.47[4]	V	
Digital supply voltage for IO pads	V_{DDP} SR	3.13	3.3	3.47 [4]	V	
VDDP voltage to ensure defined pad states[5]	V_{DDPPA} CC	0.65	–	–	V	
Digital ground voltage	V_{SS} SR	0	–	–	V	
Analog ground voltage for V_{DDM}	V_{SSM} SR	-0.1	0	0.1	V	
Analog core supply	V_{DDAF} SR	1.235	1.3	1.365[3]	V	

Table 3 Operating Conditions Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FADC / ADC analog supply voltage	V_{DDMF} SR	3.13	3.3	3.47[4)]	V	
Analog ground voltage for V_{DDMF}	V_{SSAF} SR	-0.1	0	0.1	V	

1) Applicable for digital outputs.

2) See also section ´Pin Reliability in Overload´ for overload currect definitions.

3) Voltage overshoot to 1.7V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

4) Voltage overshoot to 4.0V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.

5) This parameter is valid under the assumption the $\overline{\text{PORST}}$ signal is constantly at low level during the power-up/power-down of V_{DDP}.

Extended Range Operating Conditions

The following extended operating conditions are defined:

- 1.3V + 5% < V_{DD} / V_{DDOSC} / V_{DDAF} < 1.3V + 7.5% (overvoltage condition):
  - limited to 10000 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- 1.3V + 7.5% < V_{DD} / V_{DDOSC} / V_{DDAF} < 1.3V + 10% (overvoltage condition):
  - limited to 1 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
- V_{DDP} / V_{DDOSC3} / V_{DDFL3} / V_{DDMF}< 3.3 V ± 10%
  - 3.3V + 5% < V_{DDP} / V_{DDOSC3} / V_{DDFL3} / V_{DDMF}< 3.3V + 10% (overvoltage condition):
    limited to 1 hour duration cumulative in lifetime, due to the reliability reduction of the chip caused by the overvoltage stress.
  - 3.3V - 10% < V_{DDP} / V_{DDOSC3} / V_{DDFL3} / V_{DDMF}< 3.3 V – 5% (undervoltage condition):
    -reduces GPIO pads performance
    -no program / delete of DFLASH for T_J > 125°C
    -no program / delete of PFLASH at all

Table 4 Pin Groups for Overload / Short-Circuit Current Sum Parameter

Group	Pins
1	P5.[7:2], P5.15
2	P5.[9:8]
3	P5.[11:10]
4	P5.[14:12]
5	P1.[14:12], P2.0
6	P2.[4:1]
7	P2.[7:5]
8	P4.[2:0]
9	P4.3
10	P1.2, P1.8
11	P1.[10:9]
12	P1.3, P1.11
13	P1.[7:4]
14	P1.[1:0], P1.15
15	P3.[8:5], P3.[3:2]
16	P3.[1:0], P3.4, P3.[10:9], P3.[15:14]
17	P0.[1:0], P3.[13:11]
18	P0.[3:2], P0.[9:8]
19	P0.[11:10]
20	P6.[3:0]
21	P2.[13:8]
22	P0.[5:4], P0.[13:12]
23	P0.[7:6], P0.[15:14], P5.[1:0]

1.2 DC Parameters

1.2.1 Input/Output Pins

Table 5 Standard_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs)	C_{IO} CC	–	–	10	pF	T_A= 25 °C; f= 1 MHz
Pull-down current	$\|I_{PDL}\|$ CC	–	–	150	µA	$V_i \geq 0.6 \times V_{DDP}$ V
		10	–	–	µA	$V_i \geq 0.36 \times V_{DDP}$ V
Pull-Up current	$\|I_{PUH}\|$ CC	10	–	–	µA	$V_i \leq 0.6 \times V_{DDP}$ V
		–	–	100	µA	$V_i \leq 0.36 \times V_{DDP}$ V
Spike filter always blocked pulse duration	t_{SF1} CC	–	–	10	ns	
Spike filter pass-through pulse duration	t_{SF2} CC	100	–	–	ns	

Table 6 Standard_Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis for pads of all A classes[1)]	$HYSA$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage Current Class A1	I_{OZA1} CC	-500	–	500	nA	$V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
Ratio Vil/Vih, A1 pads	V_{ILA1} / V_{IHA1} CC	0,6	–	–		

Table 6 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the A1 pad, medium edge	R_{DSON1} CC	–	–	140	Ohm	I_{OH}< 2 mA; I_{OL}< 2 mA; P_MOS
		–	–	100	Ohm	I_{OH}< 2 mA; I_{OL}< 2 mA; N_MOS
Fall time,pad type A1	t_{FA1} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 6 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1	t_{RA1} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage class A1 pads	V_{IHA1} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3,3.6)$	V	
Input low voltage class A1 pads	V_{ILA1} SR	-0.3	–	0.36 x V_{DDP}	V	

Table 6 Standard_Pads Class_A1 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1 pads	V_{OHA1} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak
Output voltage low class A1 pads	V_{OLA1} CC	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 7 Standard_Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Leakage Current Class A1+	I_{OZA1+} CC	-1000	–	1000	nA	

Table 7 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
On-Resistance of the A1+ pad, strong soft edge	R_{DSON1+} CC	–	–	85	Ohm	I_{OH}< 2 mA; I_{OL}< 2 mA; P_MOS
		–	–	70	Ohm	I_{OH}< 2 mA; I_{OL}< 2 mA; N_MOS
Fall time, pad type A1+	t_{FA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 7 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A1+	t_{RA1+} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	28	ns	C_L= 50 pF; edge= slow ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	140	ns	C_L= 150 pF; pin out driver= medium
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, Class A1+ pads	V_{IHA1+} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3,3.6)$	V	
Input low voltage Class A1+ pads	V_{ILA1+} SR	-0.3	–	0.36 x V_{DDP}	V	

Table 7 Standard_Pads Class_A1+ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A1+ pads	V_{OHA1+} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= strong
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= strong
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak
Output voltage low class A1+ pads	V_{OLA1+} CC	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= strong
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

Table 8 Standard_Pads Class_A2

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Leakage current Class A2	I_{OZA2} CC	-6000	–	6000	nA	$V_i < V_{DDP}$ / 2 - 1 V; $V_i > V_{DDP}$ / 2 + 1 V; $V_i \geq$ 0 V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP}$ / 2 - 1 V; $V_i < V_{DDP}$ / 2 + 1 V
Ratio Vil/Vih, A2 pads	V_{ILA2} / V_{IHA2} CC	0.6	–	–		
On-Resistance of the A2 pad, strong sharp edge	R_{DSON2} CC	–	–	25	Ohm	$I_{OH} < 2$ mA; $I_{OL} < 2$ mA; P_MOS
		–	–	20	Ohm	$I_{OH} < 2$ mA; $I_{OL} < 2$ mA; N_MOS

Table 8 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time, pad type A2	t_{FA2} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	7	ns	C_L= 50 pF; edge= medium ; pin out driver= strong
		–	–	10	ns	C_L= 50 pF; edge= medium-minus ; pin out driver= strong
		–	–	3.7	ns	C_L= 50 pF; edge= sharp ; pin out driver= strong
		–	–	5	ns	C_L= 50 pF; edge= sharp-minus ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	7.5	ns	C_L= 100 pF; edge= sharp ; pin out driver= strong
		–	–	140	ns	C_L= 150 pF; pin out driver= medium

Table 8 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak

Table 8 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise time, pad type A2	t_{RA2} CC	–	–	150	ns	C_L= 20 pF; pin out driver= weak
		–	–	7.0	ns	C_L= 50 pF; edge= medium ; pin out driver= strong
		–	–	10	ns	C_L= 50 pF; edge= medium-minus ; pin out driver= strong
		–	–	3.7	ns	C_L= 50 pF; edge= sharp ; pin out driver= strong
		–	–	5	ns	C_L= 50 pF; edge= sharp-minus ; pin out driver= strong
		–	–	16	ns	C_L= 50 pF; edge= soft ; pin out driver= strong
		–	–	50	ns	C_L= 50 pF; pin out driver= medium
		–	–	7.5	ns	C_L= 100 pF; edge= sharp ; pin out driver= strong
		–	–	140	ns	C_L= 150 pF; pin out driver= medium

Table 8 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
		–	–	550	ns	C_L= 150 pF; pin out driver= weak
		–	–	18000	ns	C_L= 20000 pF; pin out driver= medium
		–	–	65000	ns	C_L= 20000 pF; pin out driver= weak
Input high voltage, class A2 pads	V_{IHA2} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3, 3.6)$	V	
Input low voltage Class A2 pads	V_{ILA2} SR	-0.3	–	0.36 x V_{DDP}	V	

Table 8 Standard_Pads Class_A2 (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output voltage high class A2 pads	V_{OHA2} CC	V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= medium
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -1.4 mA; pin out driver= strong
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= medium
		2.4	–	–	V	I_{OH}≥ -2 mA; pin out driver= strong
		V_{DDP} - 0.4	–	–	V	I_{OH}≥ -400 µA; pin out driver= weak
		2.4	–	–	V	I_{OH}≥ -500 µA; pin out driver= weak
Output voltage low class A2 pads	V_{OLA2} CC	–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= medium
		–	–	0.4	V	I_{OL}≤ 2 mA; pin out driver= strong
		–	–	0.4	V	I_{OL}≤ 500 µA; pin out driver= weak

Table 9 Standard_Pads Class_F

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis F[1]	$HYSF$ CC	0.05 x V_{DDP}	–	–	V	
Input Leakage Current Class F	I_{OZF} CC	-6000	–	6000	nA	$V_i < V_{DDP} / 2 - 1$ V; $V_i > V_{DDP} / 2 + 1$ V; $V_i \geq 0$ V; $V_i \leq V_{DDP}$ V
		-3000	–	3000	nA	$V_i > V_{DDP} / 2 - 1$ V; $V_i < V_{DDP} / 2 + 1$ V
Fall time, pad type F, CMOS mode	t_{FF2} CC	–	–	60	ns	LVDS CMOS= CMOS
Rise time, pad type F, CMOS mode	t_{RF1} CC	–	–	60	ns	LVDS CMOS= CMOS
Input high voltage, pad class F, CMOS mode	V_{IHF} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+ 0.3, 3.6)$	V	
Input low voltage, Class F pads, CMOS mode	V_{ILF} SR	-0.3	–	0.36 x V_{DDP}	V	
Output high voltage, class F pads, CMOS mode	V_{OHF} CC	$V_{DDP-0.4}$	–	–	V	$I_{OH} \geq$ -1.4 mA
		2.4	–	–	V	$I_{OH} \geq$ -2 mA
Output low voltage, class F pads, CMOS mode	V_{OLF} CC	–	–	0.4	V	$I_{OL} \leq$ 2 mA

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 10 Standard_Pads Class_I

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Hysteresis Class I[1]	$HYSI$ CC	0.1 x V_{DDP}	–	–	V	
Input Leakage Current	I_{OZI} CC	-1000	–	1000	nA	
Ratio between low and high input threshold	V_{ILI}/V_{IHI} CC	0.6	–	–		
Input high voltage, class I pins	V_{IHI} SR	0.6 x V_{DDP}	–	$min(V_{DDP}+0.3, 3.6)$	V	
Input low voltage, Class I pads	V_{ILI} SR	-0.3	–	0.36 x V_{DDP}	V	

1) Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can´t be guaranteed that it suppresses switching due to external system noise.

Table 11 LVDS_Pads Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output impedance, pad class F, LVDS mode	R_O CC	40	–	140	Ohm	
Fall time, pad type F, LVDS mode	t_{FF1} CC	–	–	2	ns	LVDS CMOS= LVDS
Rise time, pad type F, LVDS mode	t_{RF1} CC	–	–	2	ns	LVDS CMOS= LVDS
Pad set-up time	t_{SET_LVDS} CC	–	–	13	µs	
Output Differential Voltage	V_{OD} CC	150	–	400	mV	
Output voltage high, pad class F, LVDS mode	V_{OH} CC	–	–	1525	mV	
Output voltage low, pad class F, LVDS mode	V_{OL} CC	875	–	–	mV	
Output Offset Voltage	V_{OS} CC	1075	–	1325	mV	

1.2.2 Analog to Digital Converters (ADCx)

Table 12 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at the analog voltage inputs[1]	C_{AINSW} CC	–	7	20	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	25	30	pF	
Switched capacitance at the positive reference voltage input[2][3]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[2]	$C_{AREFTOT}$ CC	–	20	40	pF	
Differential Non-Linearity Error[4][5][6]	EA_{DNL} CC	-3	–	3	LSB	ADC resolution= 12-bit ; V_{DDM}= 3.3 V[7][8]
		-3	–	3	LSB	ADC resolution= 12-bit ; V_{DDM}= 5.0 V[7][8]
Gain Error[4][5][6]	EA_{GAIN} CC	-3.5	–	3.5	LSB	ADC resolution= 12-bit ; V_{DDM}= 3.3 V[7][8]
		-3.5	–	3.5	LSB	ADC resolution= 12-bit ; V_{DDM}= 5.0 V[7][8]

Table 12 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Integral Non-Linearity[4)5)6)]	EA_{INL} CC	-3	–	3	LSB	ADC resolution= 12-bit ; V_{DDM}= 3.3 V[7) 8)]
		-3	–	3	LSB	ADC resolution= 12-bit ; V_{DDM}= 5.0 V[7) 8)]
Offset Error[4)5)6)]	EA_{OFF} CC	-4	–	4	LSB	ADC resolution= 12-bit ; V_{DDM}= 3.3 V[7) 8)]
		-4	–	4	LSB	ADC resolution= 12-bit ; V_{DDM}= 5.0 V[7) 8)]
Internal ADC clock	f_{ADCI} CC	1	–	20	MHz	*reference*= VAREF ; V_{DDM}= 5.0 V
Current through resistance for the ADC test (pull-down for AIN7)	I_{AIN7T} CC	–	15	tbd	mA	
Input current at VAREF input per module[2)]	I_{AREF} CC	–	–	75	µA	$V_{AREFx} \leq V_{DDM}$ V ; $V_{AREFx} \geq$ 0 V[9)10)]

Table 12 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input leakage at analog inputs[11)]	I_{OZ1} CC	-100	–	500	nA	$V_i \leq V_{DDM}$ V; $V_i \geq 0.97 \times V_{DDM}$ V; overlayed= No
		-100	–	600	nA	$V_i \geq 0.97 \times V_{DDM}$ V; $V_i \leq V_{DDM}$ V; overlayed= Yes
		-500	–	100	nA	$V_i \leq 0.03 \times V_{DDM}$ V; $V_i \geq 0$ V; overlayed= No
		-600	–	100	nA	$V_i \leq 0.03 \times V_{DDM}$ V; $V_i \geq 0$ V; overlayed= Yes
		-100	–	200	nA	$V_i > 0.03 \times V_{DDM}$ V; $V_i < 0.97 \times V_{DDM}$ V; overlayed= No
		-100	–	300	nA	$V_i < 0.97 \times V_{DDM}$ V; $V_i > 0.03 \times V_{DDM}$ V; overlayed= Yes
Input leakage current at Varef	I_{OZ2} CC	-1	–	1	µA	$V_{AREFx} \geq 0$ V; $V_{AREFx} \leq V_{DDM}$ V
Input leakage current at Vagnd	I_{OZ3} CC	-1	–	1	µA	$V_{AGNDx} \geq 0$ V; $V_{AGNDx} \leq V_{DDM}$ V
ON resistance of the transmition gates in the analog voltage path	R_{AIN} CC	–	700	1500	Ohm	V_{DDM}= 5 V
ON resistance for the ADC test (pull down for AIN7)	R_{AIN7T} CC	180	550	900	Ohm	

Table 12 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Resistance of the reference voltage input path	R_{AREF} CC	–	500	1000	Ohm	
Total Unadjusted Error[5)6)12)]	TUE CC	-4	–	4	LSB	ADC resolution= 12-bit ; V_{DDM}= 3.3 V
		-4	–	4	LSB	ADC resolution= 12-bit ; V_{DDM}= 5.0 V
Analog reference ground[2)]	V_{AGNDx} SR	V_{SSM} - 0.05	–	V_{AREFx} - 1	V	
Analog input voltage	V_{AIN} SR	V_{AGNDx}	–	V_{DDM}	V	
Analog reference voltage[2)]	V_{AREFx} SR	V_{AGNDx} + 1	–	V_{DDM} + 0.05[13)14)]	V	
Analog reference voltage range[5)6)2)]	V_{AREFx} - V_{AGNDx} SR	V_{DDM}/2	–	V_{DDM} + 0.05	V	

1) The sampling capacity of the conversion C-network is pre-charged to V_{AREF}/2 before the sampling moment. Because of the parasitic elements the voltage measured at AINx can deviate from V_{AREF}/2.

2) Applies to AINx, when used as auxiliary reference input.

3) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead smaller capacitances are successively switched to the reference voltage.

4) The sum of DNL/INL/GAIN/OFF errors does not exceed the related TUE total unadjusted error.

5) If the analog reference voltage range is below V_{DDM} but still in the defined range of V_{DDM} / 2 and V_{DDM} is used, then the ADC converter errors increase. If the reference voltage is reduced by the factor k (k<1), TUE,DNL,INL,Gain, and Offset errors increase also by the factor 1/k.

6) If a reduced analog reference voltage between 1V and V_{DDM} / 2 is used, then there are additonal decrease in the ADC speed and accuracy.

7) For 10-bit conversions the error value must be multiplied with a factor 0.25.

8) For 8-bit conversions the error value must be multiplied with a factor 0.0625.

9) I_{AREF_MAX} is valid for the minimum specified conversion time. The current flowing during an ADC conversion with a duration of up to t_c = 25 µs can be calculated with the formula $I_{AREF\_MAX} = Q_{CONV}/t_c$. Every conversion needs a total charge of Q_{CONV} = 150 pC from V_{AREF}.

10) All ADC conversions with a duration longer than t_c = 25µs consume an I_{AREF_MAX} = 6µA.

11) The leakage current definition is a continous function,as shown in figure ADCx Analoge Input Leakage. The numerical values defined determine the characteristic points of the given countinuous linear approximation - they do not define step function.

12) Measured without noise.

13) A running conversion may become inexact in case of violating the normal conditions (voltage overshoot).

14) If the reference voltage V_{AREF} increase or the V_{DDM} decrease, so that V_{AREF} = (V_{DDM} + 0.05V to V_{DDM} + 0.07V), then the accuracy of the ADC decrease by 4LSB12.

Table 13 Conversion Time (Operating Conditions apply)

Parameter	Symbol	Values	Unit	Note
Conversion time with post-calibration	t_C CC	$2 \times T_{ADC} + (4 + STC + n) \times T_{ADCI}$	µs	n = 8, 10, 12 for n - bit conversion $T_{ADC} = 1 / f_{FPI}$ $T_{ADCI} = 1 / f_{ADCI}$
Conversion time without post-calibration		$2 \times T_{ADC} + (2 + STC + n) \times T_{ADCI}$		

The power-up calibration of the ADC requires a maximum number of 4352 f_{ADCI} cycles.

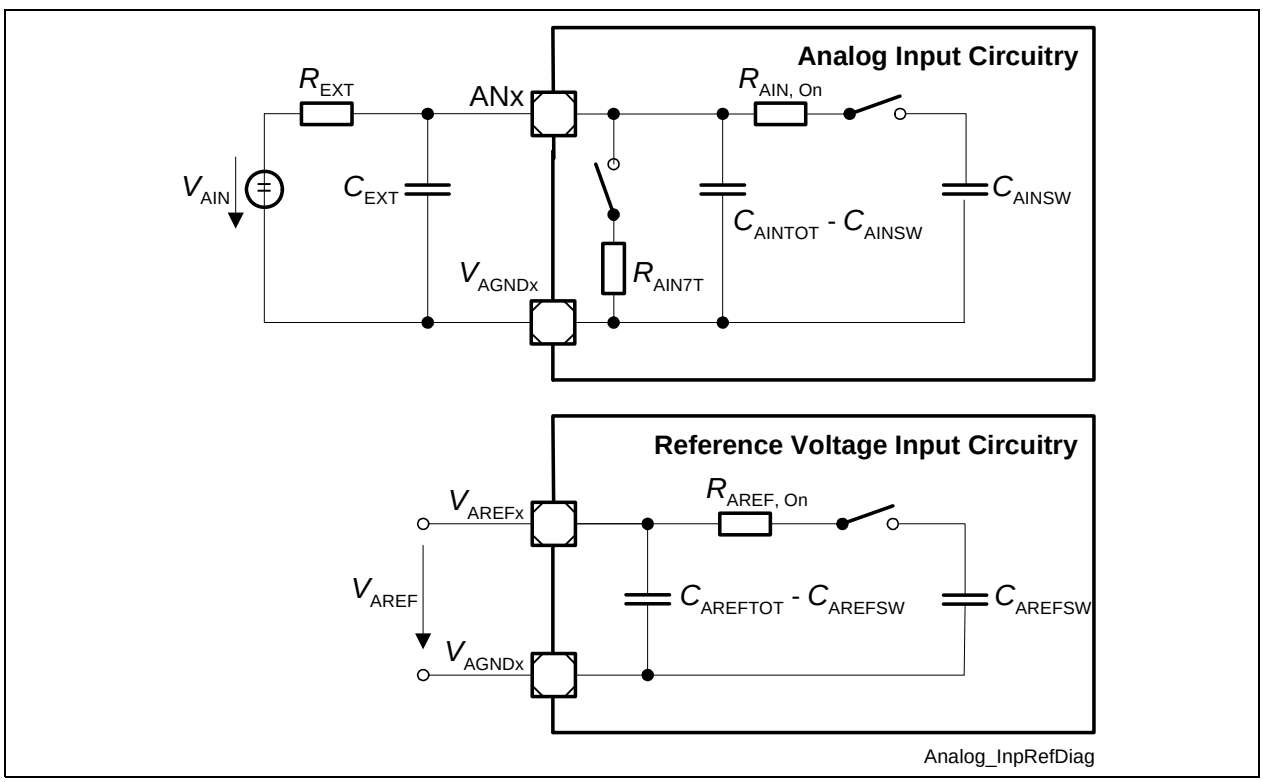


Figure 1 ADCx Input Circuits

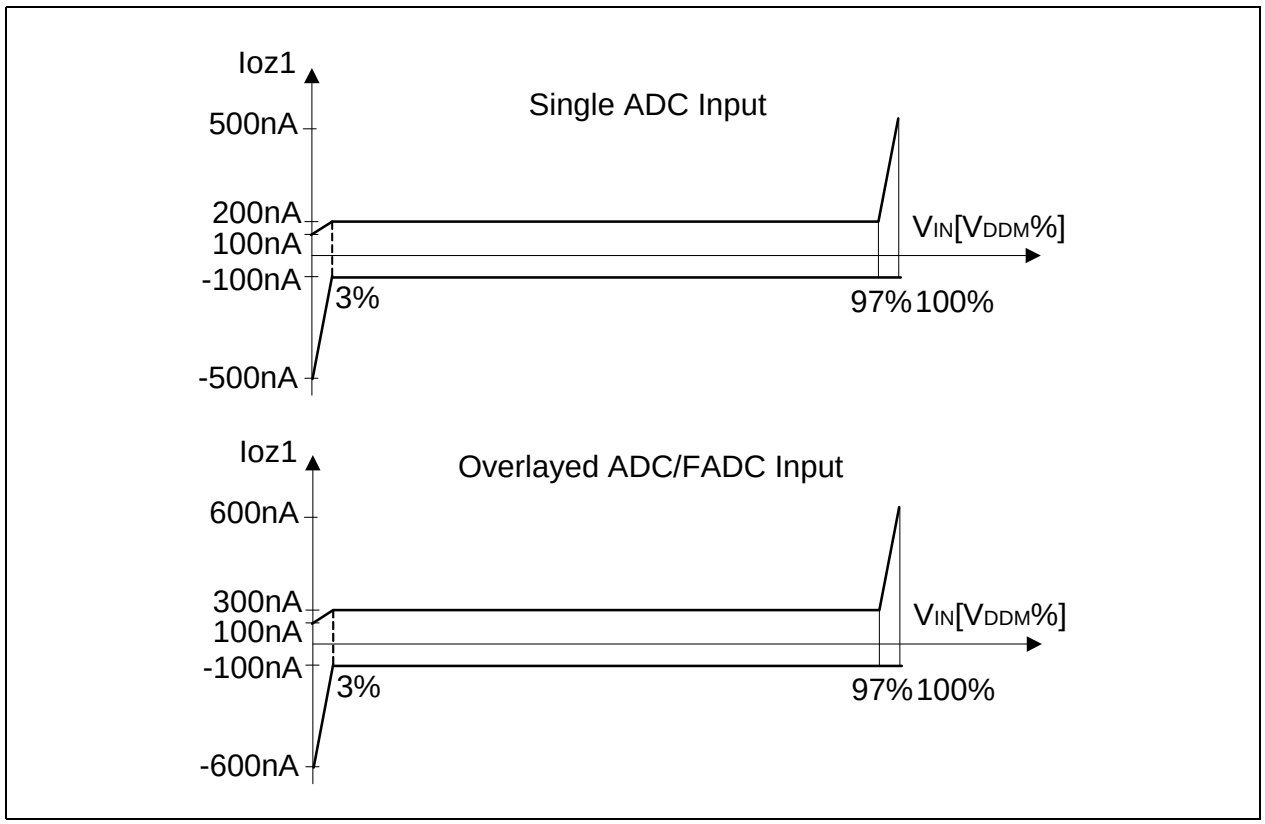


Figure 2 ADCx Analog Inputs Leakage

1.2.3 Fast Analog to Digital Converter (FADC)

Table 14 FADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at each VFAREF	I_{FAREF} CC	–	–	120	µA	
Input leakage current at VFAREF[1)]	I_{FOZ2} CC	-500	–	500	nA	$V_{FAREF} \leq V_{DDMF}$ V; $V_{FAREF} \geq 0$ V
Input leakage current at VFAGND	I_{FOZ3} CC	-8	–	8	µA	
DNL error	EF_{DNL} CC	-1	–	1	LSB	V_{IN} mode= differential
		-1	–	1	LSB	V_{IN} mode= single ended
GRADient error	EF_{GRAD} CC	-5	–	5	%	V_{IN} mode= differential ; Calibration= No ; Gain≤ 4
		-5	–	5	%	V_{IN} mode= single ended ; Calibration= No ; Gain≤ 4
		-6	–	6	%	V_{IN} mode= differential ; Calibration= No ; Gain= 8
		-6	–	6	%	V_{IN} mode= single ended ; Calibration= No ; Gain= 8
INL error	EF_{INL} CC	-4	–	4	LSB	V_{IN} mode= differential
		-4	–	4	LSB	V_{IN} mode= single ended

Table 14 FADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error	EF_{OFF} CC	-90	–	90	mV	V_{IN} mode= differential ; Calibration= No 2)
		-90	–	90	mV	V_{IN} mode= single ended ; Calibration= No 2)
		-20	–	20	mV	V_{IN} mode= differential ; Calibration= Yes 3)4)2)
		-20	–	20	mV	V_{IN} mode= single ended ; Calibration= Yes 3)4)2)
Reference error of internal VFAREF/2	EF_{REF} CC	-60	–	60	mV	
Channel amplifier cutoff frequency	f_{COFF} CC	2	–	–	MHz	
Input resistance of the analog voltage path (Rn, Rp)	R_{FAIN} CC	100	–	200	kOhm	
Settling time of a channel amplifier after changing ENN or ENP	t_{SET} CC	–	–	5	µs	
Analog input voltage range	V_{AINF} SR	V_{FAGND}	–	V_{DDMF}	V	
Analog reference ground	V_{FAGND} SR	V_{SSAF} - 0.05	–	V_{SSAF} + 0.05	V	
Analog reference voltage	V_{FAREF} SR	3.0	–	3.63 5) 6)	V	

1) This value applies in power-down mode.

2) Applies when the gain of the channel equals one. For the other gain settings, the offset error increases; it must be mulitplied with the applied gain.

3) Calibration should be preformed at each power-up. In case of a continous operation, it should be performed minimium once per week.
4) The offser error voltage drifts over the whole temperature range maximum +-3LSB.
5) Voltage overshoot to 4V is permissible, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h.
6) A running conversion may become inexact in case of violating the nomal operating conditions (voltage overshoots).

The calibration procedure should run after each power-up, when all power supply voltages and the reference voltage have stabilized.

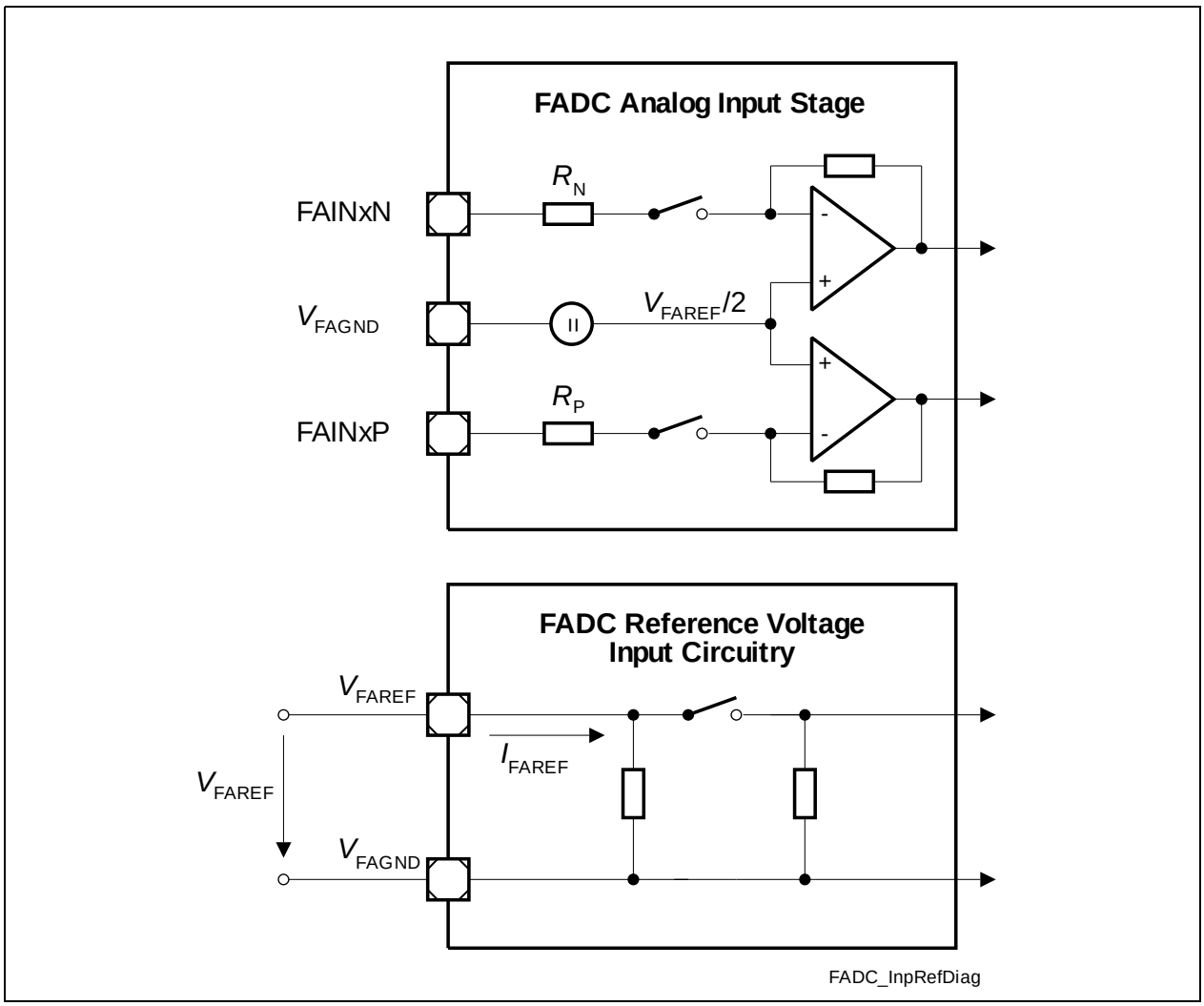


Figure 3 FADC Input Circuits

1.2.4 Oscillator Pins

Table 15 OSC_XTAL Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input current at XTAL1	I_{IX1} CC	-25	–	25	µA	$V_{IN}<V_{DDOSC3}$; $V_{IN}>0$ V
Input frequency	f_{OSC} SR	4	–	40	MHz	Direct Input Mode selected
		8	–	25	MHz	External Crystal Mode selected
Oscillator start-up time[1)]	t_{OSCS} CC	–	–	10	ms	
Input high voltage at XTAL1[2)]	V_{IHX} SR	0.7 x V_{DDOSC3}	–	V_{DDOSC3} + 0.2	V	
Input low voltage at XTAL1	V_{ILX} SR	-0.2	–	0.3 x V_{DDOSC3}	V	

1) t_{OSCS} is defined from the moment when V_{DDOSC3} = 3.13V until the oscillations reach an amplitude at XTAL1 of 0.3 * V_{DDOSC3}. The external oscillator circuitry must be optimized by the customer and checked for negative resistance as recommended and specified by crystral suppliers.

2) If the XTAL1 pin is driven by a crystal, reaching a minimum amplitude (peak-to-peak) of 0.4 * V_{DDOSC3} is necessary.

Note: It is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimal parameters for the oscillator operation. Please refer to the limits specified by the crystal or ceramic resonator supplier.

1.2.5 Temperature Sensor

Table 16 DTS Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	100	µs	
Temperature sensor range	T_{SR} SR	-40	–	150	°C	
Sensor Accuracy (calibrated)	T_{TSA} CC	-6	–	6	°C	$T_J \leq$ 120 °C
		-3	–	3	°C	$T_J >$ 120 °C
Start-up time after resets inactive	t_{TSST} SR	–	–	20	µs	

The following formula calculates the temperature measured by the DTS in [°C] from the RESULT bit field of the DTSSTAT register.

(1)

tbd

1.2.6 Power Supply Current

The total power supply current defined below consists of leakage and switching component.

Application relevant values are typically lower than those given in the following two tables and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

The operating conditions for the parameters in the following table are:
V_{DD}=1.365 V, V_{DDP}=3.47 V, f_{LMB}=180 / 133 MHz, T_J=150 °C

Table 17 Power Supply Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Core active mode supply current[1)2)]	I_{DD} CC	–	–	595[3)]	mA	power pattern= max ; *product*= SAK-TC1782-256F 133HL
		–	–	670[3)]	mA	power pattern= max ; *product*= SAK-TC1782-320F 180HL
		–	–	480[4)]	mA	power pattern= realistic ; *product*= SAK-TC1782-256F 133HL
		–	–	542[4)]	mA	power pattern= realistic ; *product*= SAK-TC1782-320F 180HL
I_{DD} current at PORST Low	I_{DD_PORST} CC	–	–	180	mA	

Table 17 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Flash memory current during continuously erasing-verifying the Flash memory[5]	I_{DDFL3E} CC	–	–	61[6]	mA	
Flash memory current during continuously reading the Flash memory[5]	I_{DDFL3R} CC	–	–	56	mA	V_{DDP}= 3.47 V
ADC 5V power supply current	I_{DDM} CC	–	–	2	mA	
FADC analog supply current, 3.3V	I_{DDMF} CC	–	–	15	mA	
Oscillator core supply current	I_{DDOSC} CC	–	–	4	mA	
Oscillator power supply current, 3.3V	I_{DDOSC3} CC	–	–	15	mA	
Pad current relevant for thermal calculation, no pad activity, LVDS off	I_{DDP} CC	–	–	15	mA	
I_{DDP} current during flash memory programming and erasing[5][7]	I_{DDP_FP} CC	–	–	55	mA	
I_{DD} current at PORST Low	I_{DDP_PORST} CC	–	–	2	mA	
Current Consumption of LVDS Pad Pairs	I_{LVDS} CC	–	–	24	mA	

Table 17 Power Supply Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum power dissipation	*PD* CC	–	–	1230	mW	power pattern= max ; *product*= SAK-TC1782-256F 133HL
		–	–	1333	mW	power pattern= max ; *product*= SAK-TC1782-320F 180HL
		–	–	1042	mW	power pattern= realistic ; *product*= SAK-TC1782-256F 133HL
		–	–	1124	mW	power pattern= realistic ; *product*= SAK-TC1782-320F 180HL
Thermal resistance junction to ambient	R_{THJA} CC	–	–	tbd	K/W	package= PG-LQFP-176-x
Analog core supply current	I_{DDAF} CC	–	–	17	mA	

1) Infineon Power Loop: CPU and PCP running, all peripherals active. The power consumption of each customer application will most probably be lower than this value, but must be evaluated seperately.
2) This current includes the E-Ray module power consumption, including the PCP operation component.
3) The I_{DD} decreases typically by 83mA if the f_{CPU} decreases by 50MHz, at constant T_J
4) The I_{DD} decreases typically by 65mA if the f_{CPU} decreases by 50MHz, at constant T_J
5) Relevant for the power supply dimensioning, not for thermal considerations.
6) In case of erase of Program Flash PF0, internal flash array loading effects may generate transient current spikes of up to 100 mA for maximum 5 ms.
7) The currenty caused by the GPIO activity depend on the particular application and should be added seperately.

1.3 AC Parameters

All AC parameters are defined with the temperature compensation disabled. That means, keeping the pads constantly at maximum strength.

1.3.1 Testing Waveforms

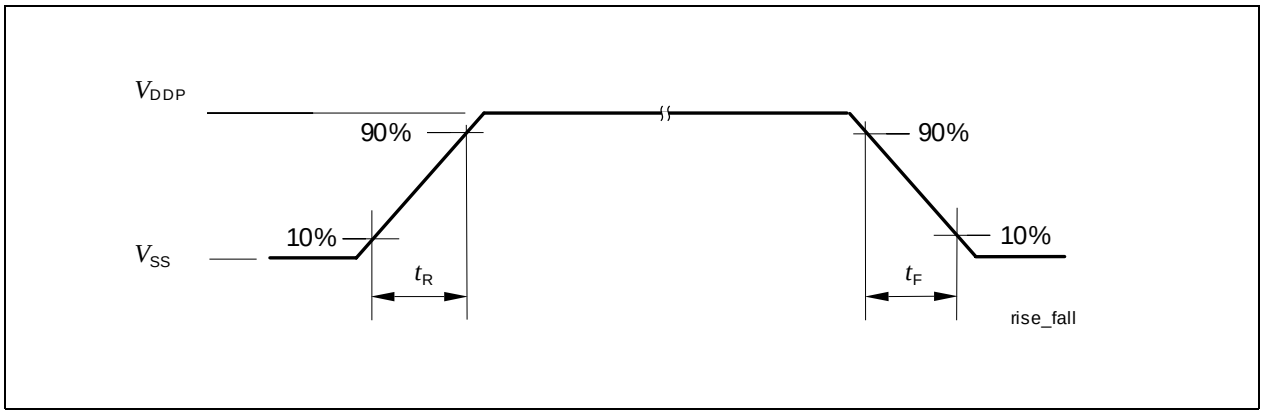


Figure 4 Rise/Fall Time Parameters

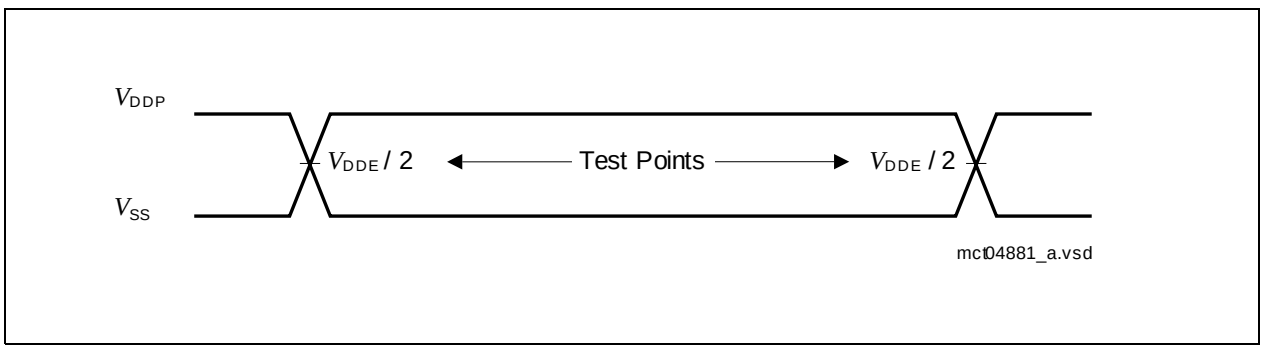


Figure 5 Testing Waveform, Output Delay

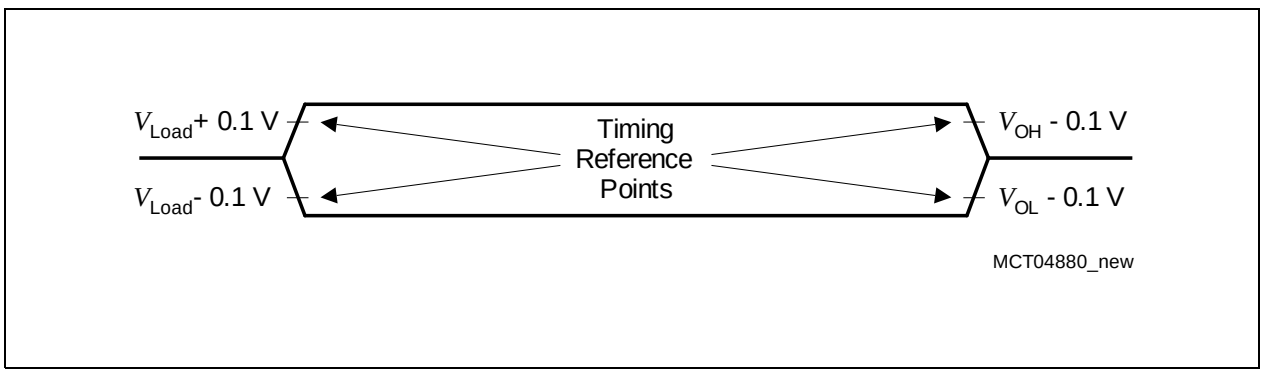


Figure 6 Testing Waveform, Output High Impedance

1.3.2 Power Sequencing

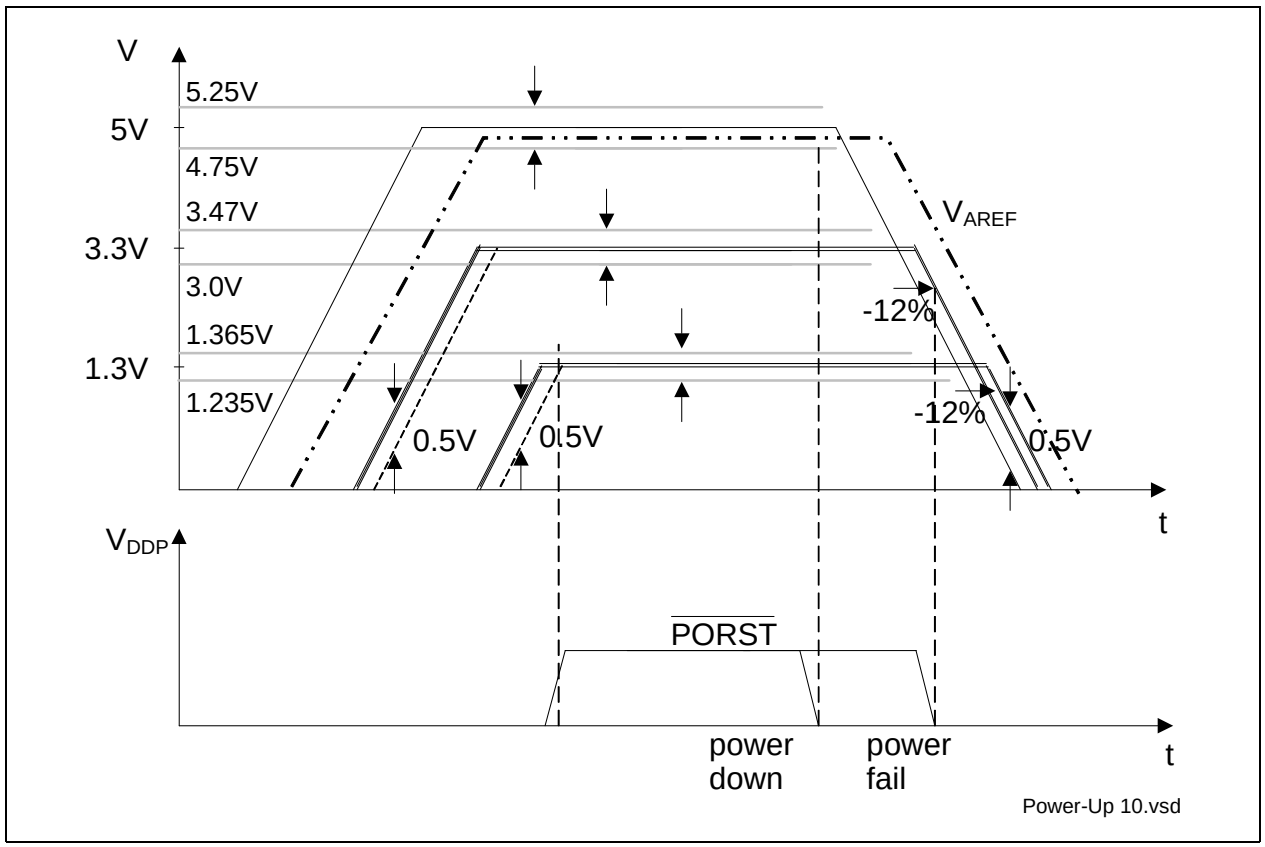


Figure 7 5 V / 3.3 V / 1.3 V Power-Up/Down Sequence

The following list of rules applies to the power-up/down sequence:

- All ground pins V_{SS} must be externally connected to one single star point in the system. Regarding the DC current component, all ground pins are internally directly connected.
- At any moment in time to avoid increased latch-up risk,
  each power supply must be higher then any lower_power_supply - 0.5 V, or:
  $V_{DD5} > V_{DD3.3} - 0.5$ V; $V_{DD5} > V_{DD1.3} - 0.5$ V;$V_{DD3.3} > V_{DD1.3} - 0.5$ V, see **Figure 7**.
  – The latch-up risk is minimized if the I/O currents are limited to:
  – 20 mA for one pin group
  – AND 100 mA for the completed device I/Os
  – AND additionally before power-up / after power-down:
  1 mA for one pin in inactive mode (0 V on all power supplies)
- During power-up and power-down, the voltage difference between the power supply pins of the same voltage (3.3 V, 1.3 V, and 5 V) with different names (for example V_{DDP}, V_{DDFL3} ...), that are internally connected via diodes, must be lower than 100 mV. On the other hand, all power supply pins with the same name (for example all V_{DDP}),

are internally directly connected. It is recommended that the power pins of the same voltage are driven by a single power supply.

1. The $\overline{\text{PORST}}$ signal may be deactivated after all V_{DD5}, $V_{DD3.3}$, $V_{DD1.3}$, and V_{AREF} power-supplies and the oscillator have reached stable operation, within the normal operating conditions.
2. At normal power down the $\overline{\text{PORST}}$ signal should be activated within the normal operating range, and then the power supplies may be switched off. Care must be taken that all Flash write or delete sequences have been completed.
3. At power fail the $\overline{\text{PORST}}$ signal must be activated at latest when any 3.3 V or 1.3 V power supply voltage falls 12% below the nominal level. If, under these conditions, the PORST is activated during a Flash write, only the memory row that was the target of the write at the moment of the power loss will contain unreliable content. In order to ensure clean power-down behavior, the $\overline{\text{PORST}}$ signal should be activated as close as possible to the normal operating voltage range.
4. In case of a power-loss at any power-supply, all power supplies must be powered-down, conforming at the same time to the rules number 2 and 4.
5. Although not necessary, it is additionally recommended that all power supplies are powered-up/down together in a controlled way, as tight to each other as possible.
6. Additionally, regarding the ADC reference voltage V_{AREF}:
   – V_{AREF} must power-up at the same time or later then V_{DDM}, and
   – V_{AREF} must power-down either earlier or at latest to satisfy the condition $V_{AREF} < V_{DDM} + 0.5$ V. This is required in order to prevent discharge of V_{AREF} filter capacitance through the ESD diodes through the V_{DDM} power supply. In case of discharging the reference capacitance through the ESD diodes, the current must be lower than 5 mA.

1.3.3 Power, Pad and Reset Timing

Table 18 Reset Timings Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Application Reset Boot Time[1)2)]	t_B CC	150	–	810	µs	*product*= SAK-TC1782-256F 133HL
		150	–	665	µs	*product*= SAK-TC1782-320F 180HL
Power on Reset Boot Time[3)4)]	t_{BP} CC	–	–	2.5	ms	
HWCFG pins hold time from ESR0 rising edge	t_{HDH} SR	16 / f_{FPI}	–	–	ns	
HWCFG pins setup time to ESR0 rising edge	t_{HDS} CC	0	–	–	ns	
Ports inactive after ESR0 reset active	t_{PI} CC	–	–	8 / f_{FPI}	ns	
Ports inactive after PORST reset active[5)]	t_{PIP} CC	–	–	150	ns	
Minimum PORST active time after power supplies are stable at operating levels	t_{POA} CC	10	–	–	ms	
Hold time from PORST rising edge	t_{POH} SR	100	–	–	ns	
PORST rise time	t_{POR} SR	–	–	50	ms	
Setup time to PORST rising edge	t_{POS} SR	0	–	–	ns	

1) The duration of the boot time is defined between the rising edge of the internal application reset and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

2) The given time includes the time of the internal reset extension for a configured value of SCU_RSTCNTCON.RELSA = 0x05BE.

3) The duration of the boot time is defined between the rising edge of the $\overline{\text{PORST}}$ and the clock cycle when the first user instruction has entered the CPU pipeline and its processing starts.

4) The given time includes the internal reset extension time for the System and Application Reset which is visible through ESR0.
5) This parameter includes the delay of the analog spike filter in the $\overline{\text{PORST}}$ pad.

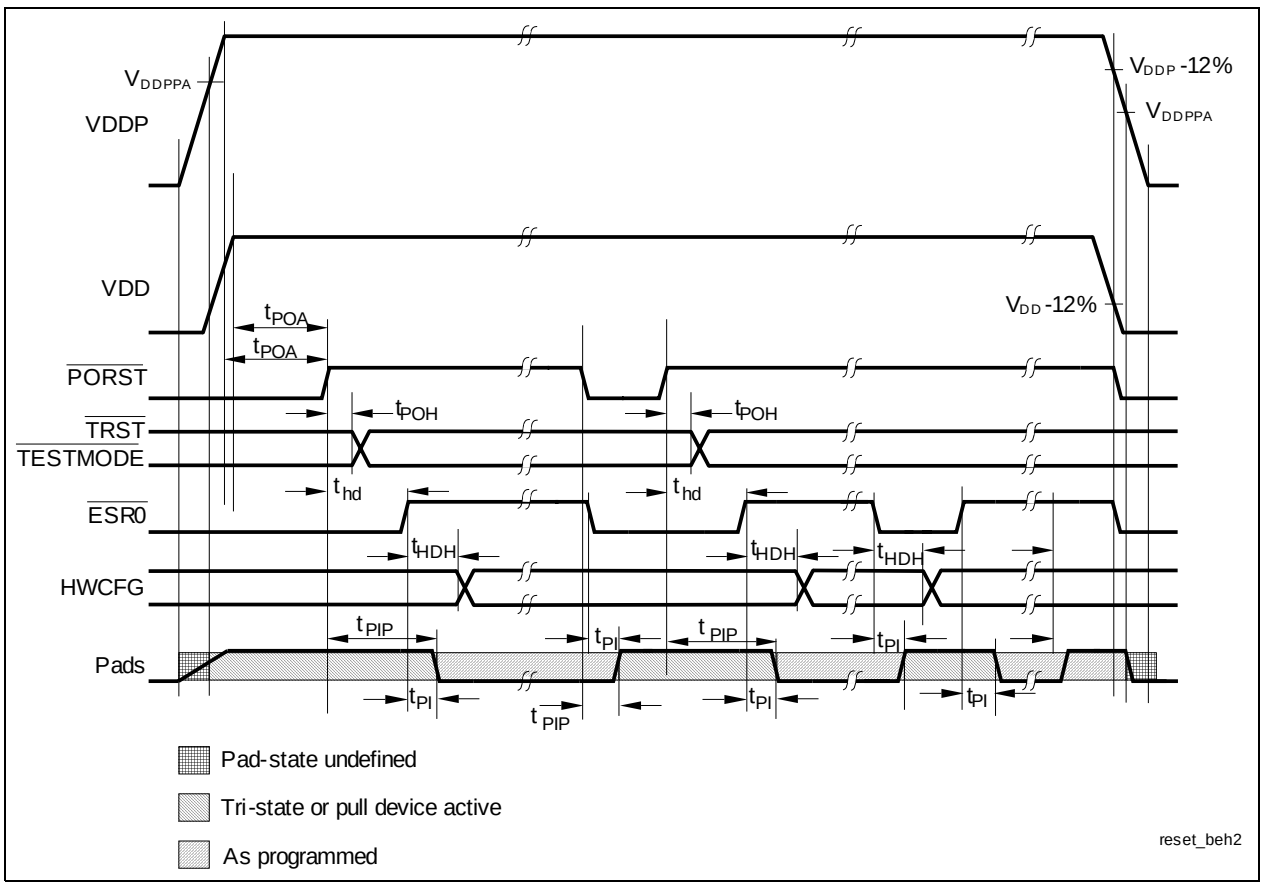


Figure 8 Power, Pad and Reset Timing

1.3.4 Phase Locked Loop (PLL)

Table 19 PLL_SysClk Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated Jitter	D_P CC	-7	–	7	ns	
PLL base frequency	$f_{PLLBASE}$ CC	50	200	320	MHz	
VCO input frequency	f_{REF} CC	8	–	16	MHz	
VCO frequency range	f_{VCO} CC	400	–	720	MHz	
PLL lock-in time	t_L CC	–	–	200	µs	

Phase Locked Loop Operation

When PLL operation is enabled and configured, the PLL clock f_{VCO} (and with it the LMB-Bus clock f_{LMB}) is constantly adjusted to the selected frequency. The PLL is constantly adjusting its output frequency to correspond to the input frequency (from crystal or clock source), resulting in an accumulated jitter that is limited. This means that the relative deviation for periods of more than one clock cycle is lower than for a single clock cycle.

This is especially important for bus cycles using wait states and for the operation of timers, serial interfaces, etc. For all slower operations and longer periods (e.g. pulse train generation or measurement, lower baudrates, etc.) the deviation caused by the PLL jitter is negligible.

Two formulas are defined for the (absolute) approximate maximum value of jitter D_m in [ns] dependent on the K2 - factor, the LMB clock frequency f_{LMB} in [MHz], and the number m of consecutive f_{LMB} clock periods.

$$\text{for} \quad (K2 \le 100) \quad \text{and} \quad (m \le (f_{LMB}[MHz])/2)$$

$$|Dm[ns]| = \left(\frac{740}{K2 \times f_{LMB}[MHz]} + 5\right) \times \left(\frac{(1 - 0,01 \times K2) \times (m - 1)}{0,5 \times f_{LMB}[MHz] - 1} + 0,01 \times K2\right) \quad (2)$$

$$\text{else} \quad |Dm[ns]| = \frac{740}{K2 \times f_{LMB}[MHz]} + 5 \quad (3)$$

With rising number m of clock cycles the maximum jitter increases linearly up to a value of m that is defined by the K2-factor of the PLL. Beyond this value of m the maximum

accumulated jitter remains at a constant value. Further, a lower LMB-Bus clock frequency f_{LMB} results in a higher absolute maximum jitter value.

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} and V_{SSOSC}, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.
The maximum peak-to peak noise on the pad supply voltage, measured between V_{DDOSC} and V_{SSOSC}, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.
These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

Oscillator Watchdog (OSC_WDT)

The expected input frequency is selected via the bit field SCU_OSCCON.OSCVAL. The OSC_WDT checks for too low frequencies and for too high frequencies.

The frequency that is monitored is f_{OSCREF} which is derived for f_{OSC}.

(4)

$$f_{OSCREF} = \frac{f_{OSC}}{OSCVAL + 1}$$

The divider value SCU_OSCCON.OSCVAL has to be selected in a way that f_{OSCREF} is 2.5 MHz.

Note: f_{OSCREF} has to be within the range of 2 MHz to 3 MHz and should be as close as possible to 2.5 MHz.

The monitored frequency is too low if it is below 1.25 MHz and too high if it is above 7.5 MHz. This leads to the following two conditions:

- Too low: f_{OSC} < 1.25 MHz × (SCU_OSCCON.OSCVAL+1)
- Too high: f_{OSC} > 7.5 MHz × (SCU_OSCCON.OSCVAL+1)

Note: The accuracy is 30% for these boundaries.

1.3.5 ERAY Phase Locked Loop (ERAY_PLL)

Table 20 PLL_ERAY Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Accumulated jitter at SYSCLK pin	D_{PP} CC	-0.8	–	0.8	ns	
Accumulated_Jitter	D_P CC	-0.5	–	0.5	ns	
PLL Base Frequency of the ERAY PLL	$f_{PLLBASE\_ERAY}$ CC	50	200	360	MHz	
VCO input frequency of the ERAY PLL	f_{REF} CC	20	–	40	MHz	
VCO frequency range of the ERAY PLL	f_{VCO_ERAY} CC	450	–	500	MHz	
PLL lock-in time	t_L CC	–	–	200	µs	

Note: The specified PLL jitter values are valid if the capacitive load per pin does not exceed C_L = 20 pF with the maximum driver and sharp edge.

Note: The maximum peak-to-peak noise on the pad supply voltage, measured between V_{DDOSC3} and V_{SSOSC}, is limited to a peak-to-peak voltage of V_{PP} = 100 mV for noise frequencies below 300 KHz and V_{PP} = 40 mV for noise frequencies above 300 KHz.
These conditions can be achieved by appropriate blocking of the supply voltage as near as possible to the supply pins and using PCB supply and ground planes.

1.3.6 JTAG Interface Timing

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 21 JTAG Interface Timing Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	25	–	–	ns	–
TCK high time	t_2 SR	10	–	–	ns	–
TCK low time	t_3 SR	10	–	–	ns	–
TCK clock rise time	t_4 SR	–	–	4	ns	–
TCK clock fall time	t_5 SR	–	–	4	ns	–
TDI/TMS setup to TCK rising edge	t_6 SR	6	–	–	ns	–
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	–
TDO valid after TCK falling edge[1] (propagation delay)	t_8 CC	–	–	13	ns	C_L = 50 pF
	t_8 CC	3	–	–	ns	C_L = 20 pF
TDO hold after TCK falling edge[1]	t_{18} CC	2	–	–	ns	
TDO high imped. to valid from TCK falling edge[1)2)]	t_9 CC	–	–	14	ns	C_L = 50 pF
TDO valid to high imped. from TCK falling edge[1]	t_{10} CC	–	–	13.5	ns	C_L = 50 pF

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

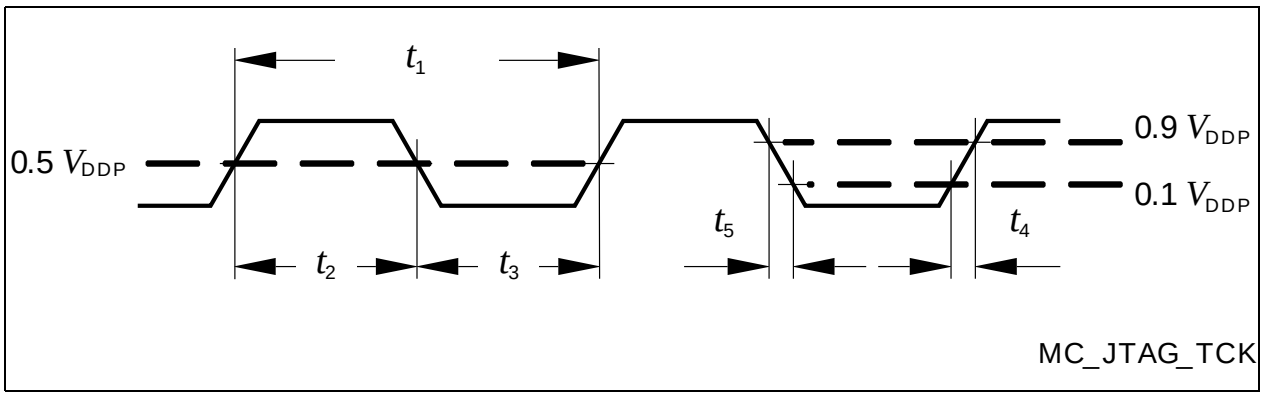


Figure 9 Test Clock Timing (TCK)

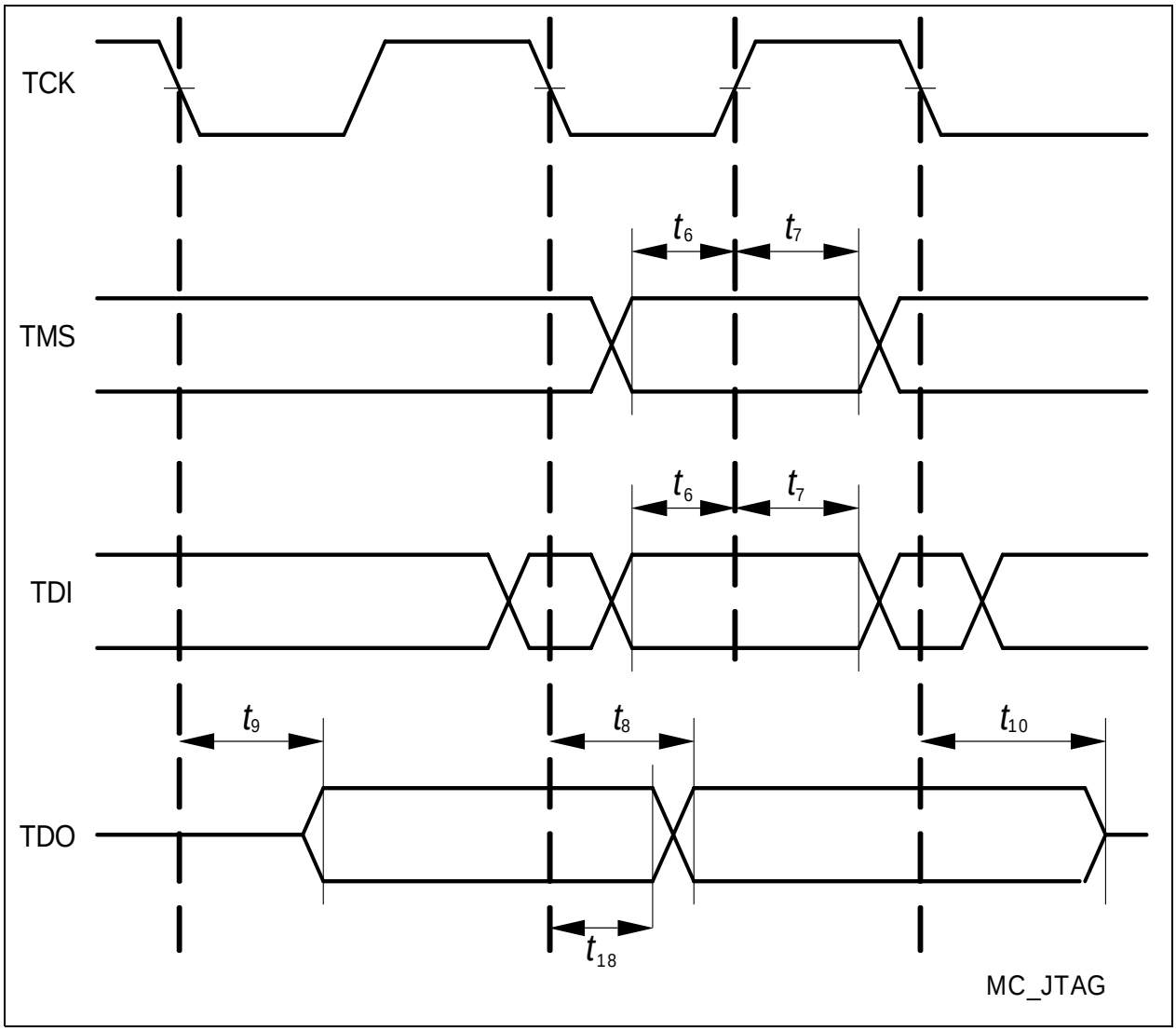


Figure 10 JTAG Timing

1.3.7 DAP Interface Timing

The following parameters are applicable for communication through the DAP debug interface.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Table 22 DAP Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DAP0 clock period[1]	t_{TCK} SR	12.5	–	–	ns	
DAP0 high time	t_{12} SR	4	–	–	ns	
DAP0 low time[1]	t_{13} SR	4	–	–	ns	
DAP0 clock rise time	t_{14} SR	–	–	2	ns	
DAP0 clock fall time	t_{15} SR	–	–	2	ns	
DAP1 setup to DAP0 rising edge	t_{16} SR	6.0	–	–	ns	
DAP1 hold after DAP0 rising edge	t_{17} SR	6.0	–	–	ns	
DAP1 valid per DAP0 clock period[2]	t_{19} SR	8	–	–	ns	C_L= 20 pF; f= 80 MHz
		10	–	–	ns	C_L= 50 pF; f= 40 MHz

1) See the DAP chapter for clock rate restrictions in the Active:IDLE protocol state.

2) The Host has to find a suitable sampling point by analyzing the sync telegram response.

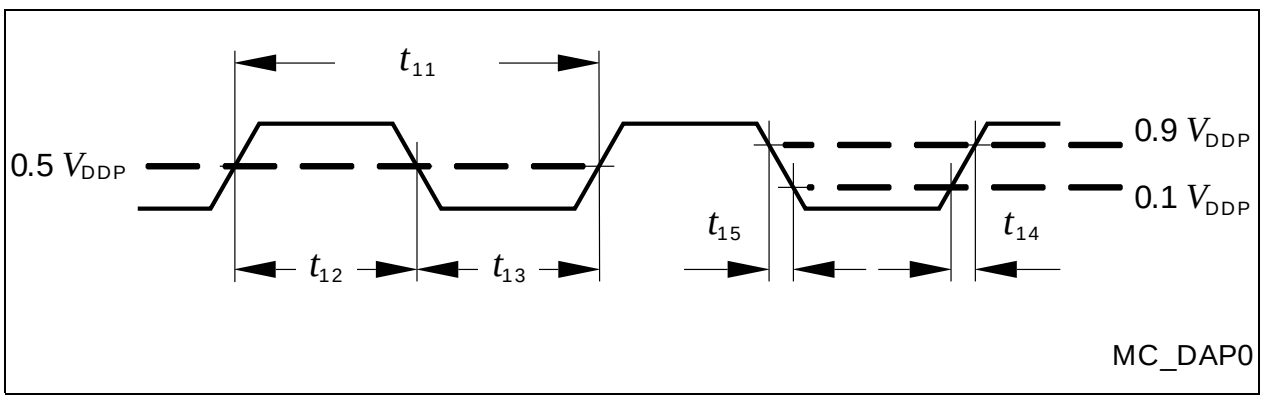


Figure 11 Test Clock Timing (DAP0)

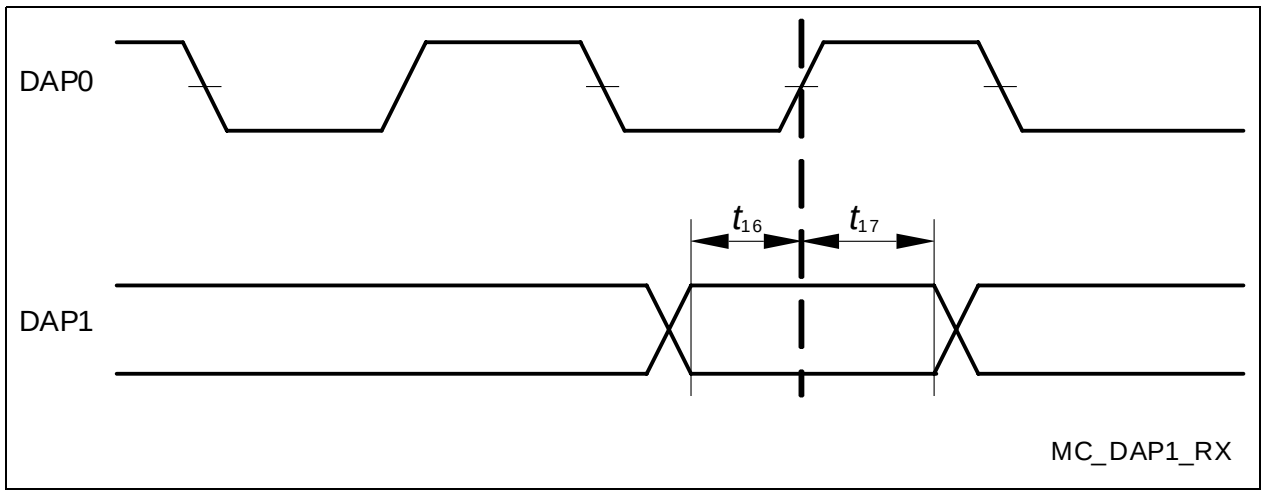


Figure 12 DAP Timing Host to Device

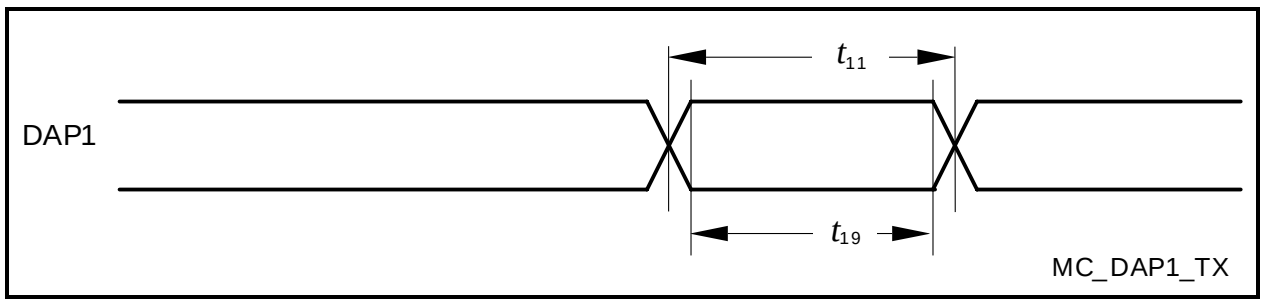


Figure 13 DAP Timing Device to Host

1.3.8 Peripheral Timings

Note: Peripheral timing parameters are not subject to production test. They are verified by design/characterization.

1.3.8.1 Micro Link Interface (MLI) Timing

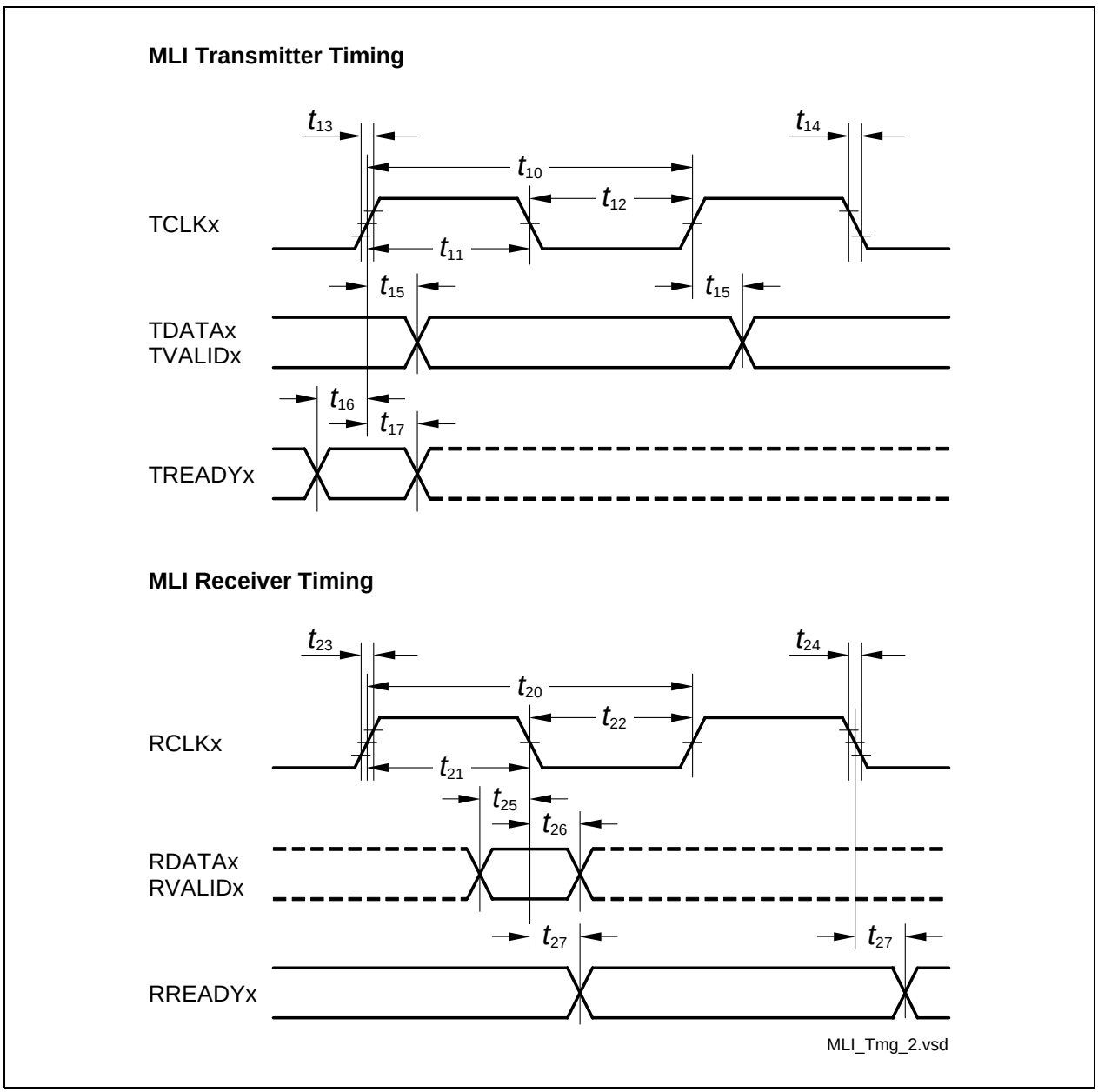


Figure 14 MLI Interface Timing

Note: The generation of RREADYx is in the input clock domain of the receiver. The reception of TREADYx is asynchronous to TCLKx.

Table 23 MLI Receiver

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RCLK clock period	t_{20} SR	1 / f_{FPI}	–	–	ns	
RCLK high time[1)2)]	t_{21} SR	–	0.5 x t_{20}	–	ns	
RCLK low time[1)2)]	t_{22} SR	–	0.5 x t_{20}	–	ns	
RCLK rise time[3)]	t_{23} SR	–	–	4	ns	
RCLK fall time[3)]	t_{24} SR	–	–	4	ns	
RDATA/RVALID setup time before RCLK falling edge	t_{25} SR	4.2	–	–	ns	
RDATA/RVALID hold time after RCLK falling edge	t_{26} CC	2.2	–	–	ns	
RREADY output delay time	t_{27} CC	0	–	16	ns	

1) The following formula is valid: t21 + t22 = t20.

2) Min and Max values for this parameter can be derived from the typ. value by considering the other receiver timing parameters.

3) The RCLK max. input rise/fall times are best case parameters for fSYS = 90 MHz. For reduction of EMI, slower input signal rise/fall times can be used for longer RCLK clock periods.

Table 24 is valid under the following conditions: edge=medium

Table 24 MLI Transmitter

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK clock period	t_{10} CC	2 x 1 / f_{FPI}	–	–	ns	
TCLK high time[1)2)]	t_{11} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK low time[1)2)]	t_{12} CC	0.45 x t_{10}	0.5 x t_{10}	0.55 x t_{10}	ns	
TCLK rise time	t_{13} CC	–	–	16[3)]	ns	

Table 24 MLI Transmitter (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCLK fall time	t_{14} CC	–	–	16[3)]	ns	
TDATA/TVALID output delay time	t_{15} CC	-3	–	4.4	ns	
TREADY setup time before TCLK rising edge	t_{16} SR	18	–	–	ns	
TREADY hold time after TCLK rising edge	t_{17} SR	-4	–	–	ns	

1) The following formula is valid: t11 + t12 = t10.

2) The min./max. TCLK low/high times t11/t12 include the PLL jitter of fSYS. Fractional divider settings must be regarded additionally to t11 / t12.

3) For high-speed MLI interface, strong driver sharp or medium edge selection (class A2 pad) is recommended for TCLK.

1.3.8.2 Micro Second Channel (MSC) Interface Timing

Table 25 MSC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
FCLP clock period[1)2)]	t_{40} CC	2 x T_{MSC}[3)]	–	–	ns	
SOP/ENx outputs delay from FCLP rising edge	t_{45} CC	-10	–	10	ns	
SDI bit time	t_{46} CC	8 x T_{MSC}	–	–	ns	
SDI rise time	t_{48} SR	–	–	100	ns	
SDI fall time	t_{49} SR	–	–	100	ns	

1) FCLP signal rise/fall times are only defined by the pad rise/fall times.

2) FCLP signal high and low can be minimum $1\xi\phi_{TMSC}$

3) TMSC = TSYS = 1 / fSYS.

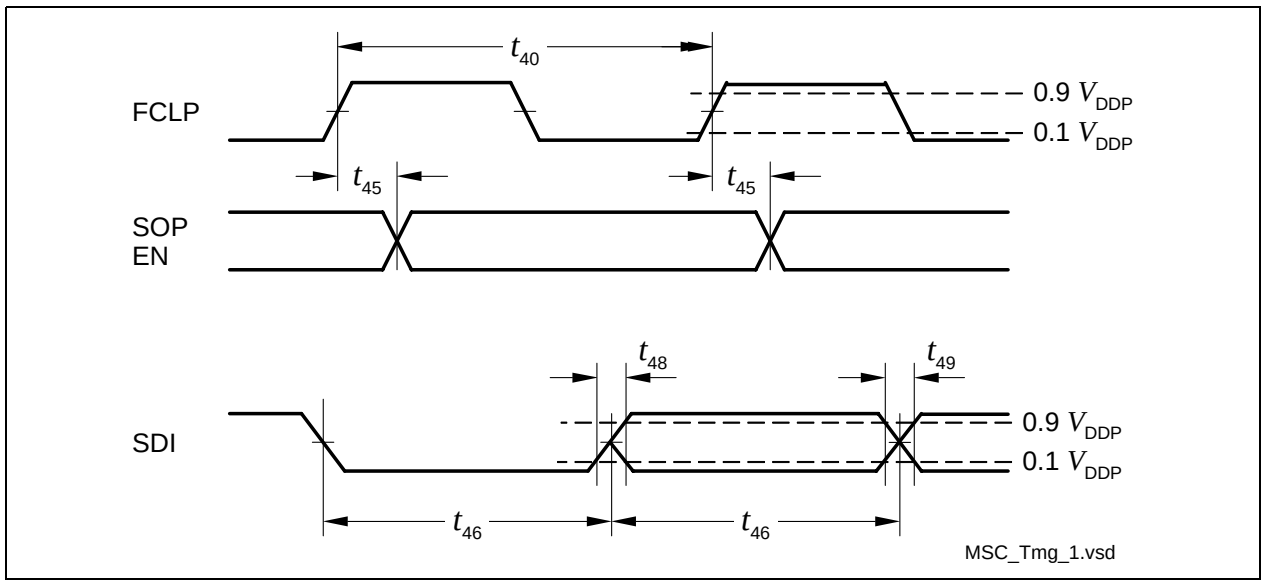


Figure 15 MSC Interface Timing

Note: The data at SOP should be sampled with the falling edge of FCLP in the target device.

1.3.8.3 SSC Master/Slave Mode Timing

Table 26 SSC Parameters

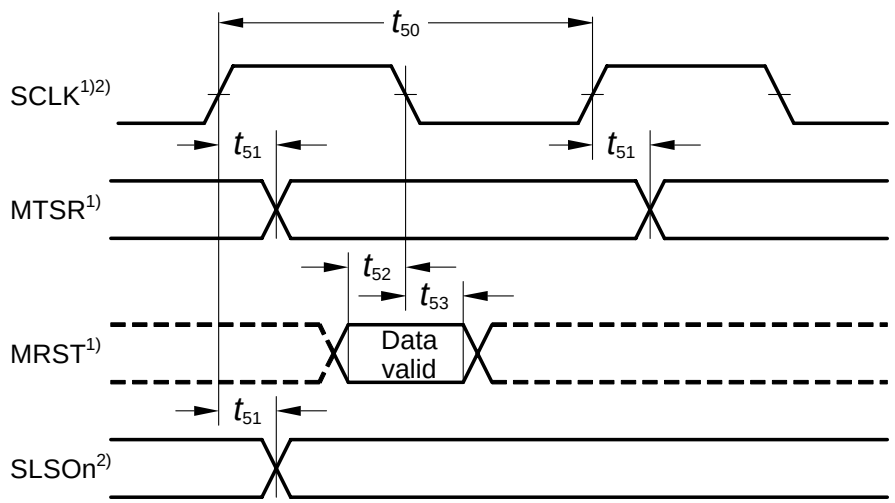
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLK clock period[1)2)3)]	t_{50} CC	2 x 1 / f_{FPI}	–	–	ns	
MTSR/SLSOx delay form SCLK rising edge	t_{51} CC	0	–	8	ns	
MRST setup to SCLK falling edge[3)]	t_{52} SR	16.5	–	–	ns	
MRST hold from SCLK falling edge[3)]	t_{53} SR	0	–	–	ns	
SCLK input clock period[1)3)]	t_{54} SR	4 x 1 / f_{FPI}	–	–	ns	
SCLK input clock duty cycle	t_{55}_t_{54} SR	45	–	55	%	
MTSR setup to SCLK latching edge[3)4)]	t_{56} CC	1 / f_{FPI}	–	–	ns	
MTSR hold from SCLK latching edge	t_{57} CC	1 / f_{FPI} + 5	–	–	ns	
SLSI setup to first SCLK latching edge	t_{58} CC	1 / f_{FPI} + 5	–	–	ns	
SLSI hold from last SCLK latching edge	t_{59} CC	7	–	–	ns	
MRST delay from SCLK shift edge	t_{60} CC	0	–	16.5	ns	
SLSI to valid data on MRST	t_{61} CC	–	–	16.5	ns	

1) SCLK signal rise/fall times are the same as the rise/fall times of the pad.

2) SCLK signal high and low times can be minimum 1xTSSC.

3) TSSCmin = TSYS = 1/fSYS.

4) Fractional divider switched off, SSC internal baud rate generation used.

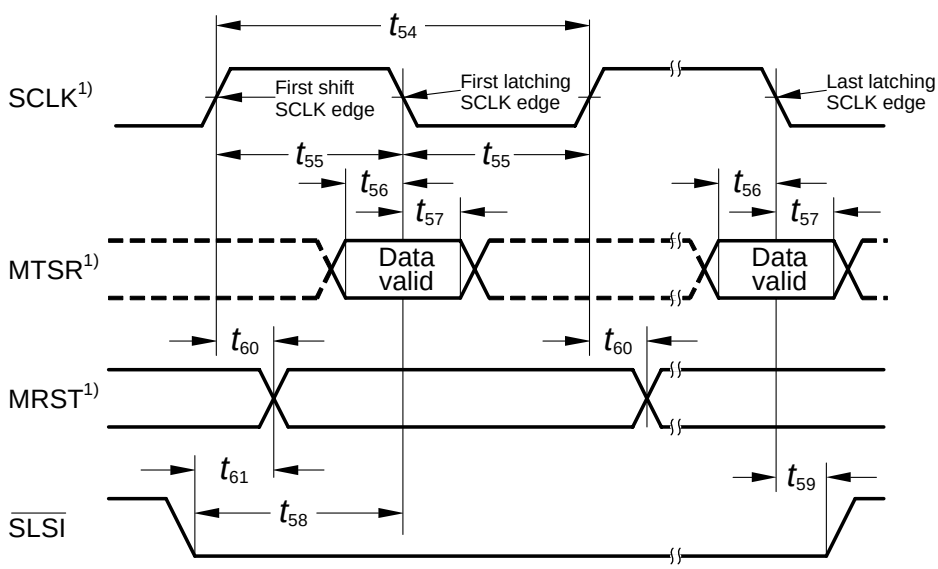


1) This timing is based on the following setup: CON.PH = CON.PO = 0.

2) The transition at SLSOn is based on the following setup: SSOTC.TRAIL = 0 and the first SCLK high pulse is in the first one of a transmission.

SSC_TmgMM

Figure 16 SSC Master Mode Timing



1) This timing is based on the following setup: CON.PH = CON.PO = 0.

SSC_TmgSM

Figure 17 SSC Slave Mode Timing

1.3.8.4 ERAY Interface Timing

C_L = 25 pF

The ERAY interface is only available for the SAK-TC1782-320F180HL.

Table 27 ERAY Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Time span from last BSS to FES without the influence of quartz tolerancies (d10Bit_TX)[1]	t_{60} CC	997.25	–	1002.25	ns	
TxD data valid from fsample flip flop txd_reg TxDA, TxDB (dTxAsym)[2][3]	t_{61}-t_{62} CC	–	–	1.5	ns	Asymmetrical delay of rising and falling edge (TxDA, TxDB)
Time span between last BSS and FES without influence of quartz tolerancies (d10Bit_RX)[1][4][5]	t_{63} SR	967	–	1046.1	ns	
RxD capture by fsample (RxDA/RxDB sampling flip-flop) (dRxAsym)[6]	t_{64}-t_{65} CC	–	–	3.0	ns	Asymmetrical delay of rising and falling edge (RxDA, RxDB)

1) This includes the PLL_ERAY accumulated jitter.

2) Refers to delays caused by the asymmetries of the output drivers of the digital logic and the GPIO pad drivers. Quarz tolerance and PLL_ERAY accumulated jitter are not included.

3) E-Ray TxD output drivers have an asymmetry of rising and falling edges of $|t_{FA2} - t_{RA2}|$ 1 ns.

4) The Min limit correspond to 30% * V_{DDP} FlexRay standard input thresholds. The Max limit correspond to 70% * V_{DDP} FlexRay standard input thresholds. Due to different input thresholds for this product, a correction of -0.5 ns and +0.1 ns has been applied.

5) Valid for output slopes of the bus driver of dRxSlope 5ns, 20% * V_{DDP} to 80% * V_{DDP}, according to the FlexRay Electrical Physical Layer Specification V2.1B. For A2 pads, the rise and fall times of the incoming signal have to satisfy the following inequality: -1.6ns $t_{FA2} - t_{RA2}$ 1.3ns.

6) Valid for output slopes of the bus driver of dRxSlope 5ns, 20% * V_{DDP} to 80% * V_{DDP}, according to the FlexRay Electrical Physical Layer Specification V2.1B. For A2 pads, the rise and fall times of the incoming signal have to satisfy the following inequality: -1.6ns $t_{FA2} - t_{RA2}$ 1.3ns.

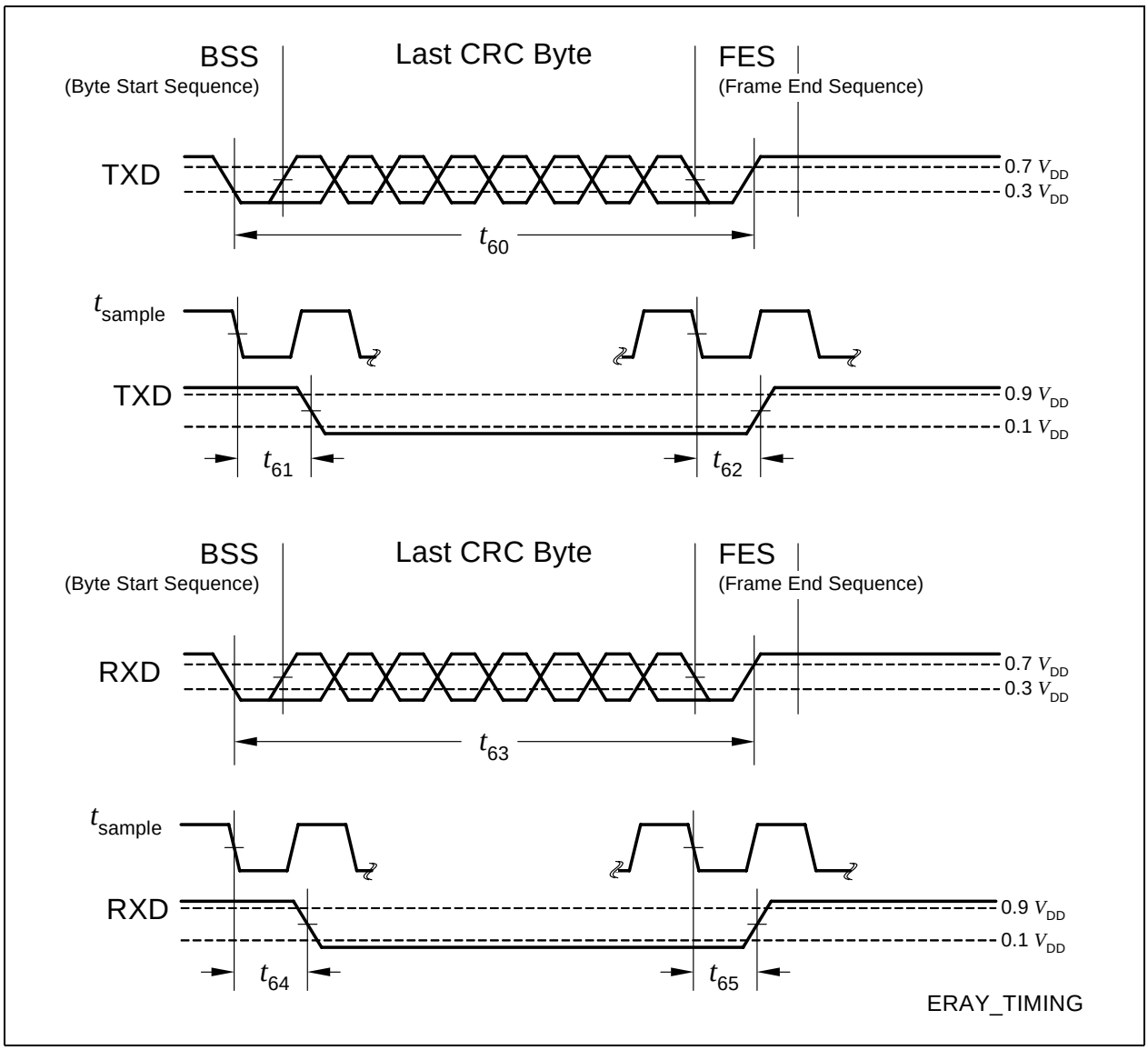


Figure 18 ERAY Timing

1.4 Package and Reliability

1.4.1 Package Parameters

Table 28 Thermal Characteristics of the Package

Device	Package	$R_{\Theta JCT}$ 1)	$R_{\Theta JCB}$ 1)	$R_{\Theta JLead}$ 2)	Unit	Note
TC1782	PG-LQFP-176-6	8,1	0,3	30,9	K/W	

1) The top and bottom thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) are to be combined with the thermal resistances between the junction and the case given above (R_{TJCT}, R_{TJCB}), in order to calculate the total thermal resistance between the junction and the ambient (R_{TJA}). The thermal resistances between the case and the ambient (R_{TCAT}, R_{TCAB}) depend on the external system (PCB, case) characteristics, and are under user responsibility.
The junction temperature can be calculated using the following equation: $T_J = T_A + R_{TJA} \times P_D$, where the R_{TJA} is the total thermal resistance between the junction and the ambient. This total junction ambient resistance R_{TJA} can be obtained from the upper four partial thermal resistances.
Thermal resistances as measured by the 'cold plate method' (MIL SPEC-883 Method 1012.1).

2) with connected ePad.

1.4.2 Package Outline

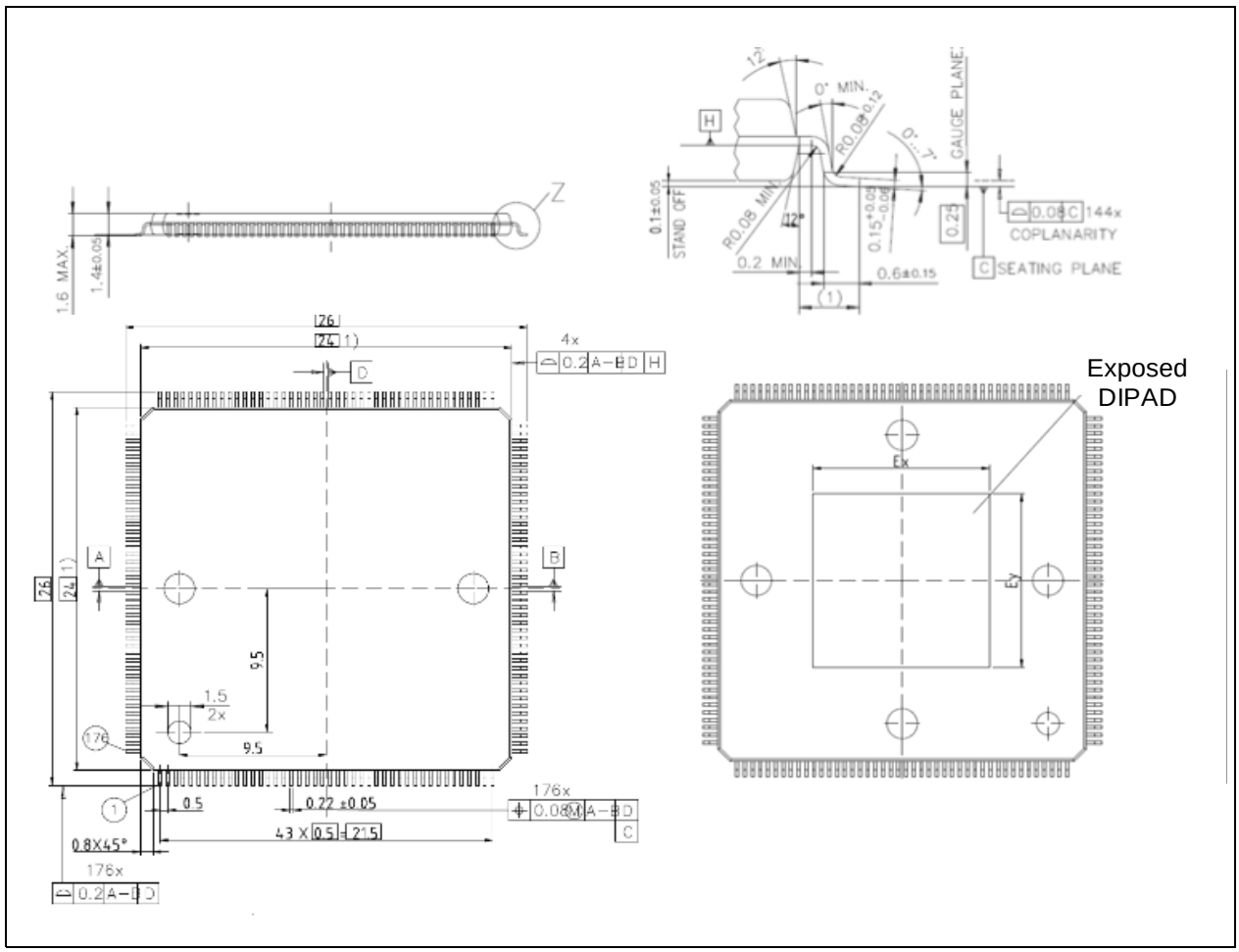


Figure 19 Package Outlines PG-LQFP-176-6

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: ***http://www.infineon.com/products***.

1.4.3 Flash Memory Parameters

The data retention time of the TC1782’s Flash memory depends on the number of times the Flash memory has been erased and programmed.

Table 29 FLASH32 Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Data Flash Erase Time per Sector	t_{ERD} CC	–	–	3	s	
Program Flash Erase Time per 256 KByte Sector	t_{ERP} CC	–	–	5	s	
Program time data flash per page[1)]	t_{PRD} CC	–	5	15	ms	
Program time program flash per page[2)]	t_{PRP} CC	–	5	10	ms	
Data Flash Endurance	N_E CC	60000 [3)]	–	–	cycles	Max. data retention time 5 years
Erase suspend delay	t_{FL_ErSusp} CC	–	–	15	ms	
Wait time after margin change	$t_{FL\_MarginDel}$ CC	10	–	–	µs	
Program Flash Retention Time, Physical Sector[4)5)]	t_{RET} CC	20	–	–	years	Max. 1000 erase/program cycles
Program Flash Retention Time, Logical Sector[4)5)]	t_{RETL} CC	20	–	–	years	Max. 100 erase/program cycles
UCB Retention Time[4)5)]	t_{RTU} CC	20	–	–	years	Max. 4 erase/program cycles per UCB
Wake-Up time	t_{WU} CC	–	–	270	µs	
DFlash wait state configuration	WS_{DF} CC	50 ns x f_{FSI}	–	–		
PFlash wait state configuration	WS_{PF} CC	26 ns x f_{FSI}	–	–		

1) In case the Program Verify feature detects weak bits, these bits will be programmed up to twice more. Each reprogramming takes additional 5 ms.

2) In case the Program Verify feature detects weak bits, these bits will be programmed once more. The reprogramming takes additional 5 ms.

3) Only valid when a robust EEPROM emulation algorithm is used. For more details see the User´s Manual.
4) Storage and inactive time included.
5) At average weighted junction temperature T_j = 100°C, or the retention time at average weighted temperature of T_j = 110°C is minimum 10 years, or the retention time at average weighted temperature of T_j = 150°C is minimum 0.7 years.

The following constraints regarding FLASH performance apply additionally for 3.0 V < V_{DDP} < 3.13 V (- 5% to - 10%) on V_{DDP} pin:
no program / delete of DFLASH for T_J > 125°C, no program / delete of PFLASH at all.

1.4.4 Quality Declarations

Table 30 Quality Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Operation Lifetime[1)]	t_{OP}	–	–	24000	hours	–[2)]
ESD susceptibility according to Human Body Model (HBM)	V_{HBM}	–	–	2000	V	Conforming to JESD22-A114-B
ESD susceptibility of the LVDS pins	V_{HBM1}	–	–	500	V	–
ESD susceptibility according to Charged Device Model (CDM)	V_{CDM}	–	–	500	V	Conforming to JESD22-C101-C
Moisture Sensitivity Level	MSL	–	–	3	–	Conforming to Jedec J-STD-020C for 240°C

1) This lifetime refers only to the time when the device is powered on.
2) For worst-case temperature profile equivalent to:
1200 hours at T_j = 125...150°C
3600 hours at T_j = 110...125°C
7200 hours at T_j = 100...110°C
11000 hours at T_j = 25...110°C
1000 hours at T_j = -40...25°C

1.5 Pin Reliability in Overload

1.5.1 Introduction

When receiving signals from the external world or higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supply. In order to design cost-optimized high-reliability systems (close to 0 ppm fail-rate in the whole lifetime), some design issues must be taken into account. This document describes these issues. They are relevant only for the overloaded input pins/pins set to input of the device/application.

There are two types of constraints for an input pad in overload: voltage and current constraints. At 3.3V low voltage CMOS devices, the voltage constraints are more critical than the current constraints. The reason for this effect is the thinner Gate Oxide layer at low-voltage devices. This effect is intrinsic to the Gate Oxide and can not be avoided.

Two general cases are discussed in this document:

- full life-time, normal operation, high/room temperature reliability (24000 h)
- limited duration, error case, high/room temperature reliability (2400 h)

1.5.1.1 Pin Classes

All TC1782 pins include internal protection diodes connected to power supply voltage and to ground. However, the voltage/current characteristics differs in case of different types of pads. There are three classes of GPIO pads, regarding their input characteristics:

- A2 - Strong Driver Pad
- A1, and Digital Inputs Only - Low Leakage Pads
- LVDS Combo Pads

Generally, the Strong Driver Class has lower protection diode voltage drop than the Low Leakage Class. This means that Strong Driver pins experience less voltage in overload then the other pins.

1.5.1.2 External Influences

Apart from the input current, two other factors influence the voltage that will appear on an input pin in overload: the power supply voltage and the die temperature.

Increasing the power supply voltage directly increases the voltage on all pins in overload. When power supply voltage would increase from nominal 3.3 V to maximal 3.47 V, voltage on all overloaded pins would increase for 0.17 V.

When the temperature goes lower, the PN-junction voltage goes higher, provided that the current remains constant. For the automotive temperature range of -40°C to +150°C

junction temperature, the voltage variations of up to 0.3 V are possible. On the other hand, Gate Oxide reliability increases at lower temperatures. Thus, the high temperature case is the worst case, although at lower temperatures the voltages are higher.

1.5.1.3 General Recommendations

The following general recommendation apply, when designing high reliability systems:

Normal operation case (full lifetime case):

1. Use the normal operation instead of overload, whenever possible.
2. Use voltage dividers to bring the voltage down to normal operating range. This is recommended for the A1 class pads and the Digital Input Only pads in full lifetime overload. This connection has a property that the pins can go no higher than the divided voltage, independently of the temperature and the power supply variations, if the divided voltage is lower than the nominal supply voltage. In other cases, consult the reliability data as listed in **Reliability Characteristics, High Temperatures**.
3. Current limiting with serial resistors only, full lifetime, for A2 class pads gives the reliability data as listed in **Reliability Characteristics, High Temperatures**.

Error case (limited duration case):

1. Limit the overload current as low as possible. Consult the reliability data as listed in **Reliability Characteristics, High Temperatures**.

Additionally:

- when interfacing signals with long idle times (interrupts, serial clocks ...) it is reasonable, whenever possible, to use the low level as the idle level.
- using power supplies with smaller static tolerance directly improves the reliability.

1.5.2 Positive Overload

1.5.2.1 Reliability at Room Temperature

The reliability data given in this document is calculated for one pin of each relevant class. The reliability of n pins is derived by multiplying the one-pin reliability with the number of pins under consideration, of each pad class separately. The high temperature case is the worst case, although the PN-junction voltages at high temperatures are the lowest.

PN Junction Characteristics

The following table gives the PN-junction voltage current dependence for Room Temperature, different pin classes.

Table 31 PN-Junction Characteristics

Class	0.2 mA	0.5 mA	1 mA	3 mA
LVDS	4.0 V	4.05 V	4.15 V	4.35 V
FADC / Digital Input	4.1 V	4.12 V	4.14 V	4.17 V
A1	3.95 V	4.06 V	4.1 V	4.15 V
A2	3.73 V	3.78 V	3.84 V	4 V

These pin overload voltages refer to the nominal power supply of V_{DDP} = 3.3 V. The maximum values are obtained, at V_{DDP} = 3.47 V, by adding 0.17 V to the values above.

Reliability Characteristics, Room Temperature

The following tables give the reliability calculated for single pin of each class, Room Temperature, total life-time 24000h. The reliability is expressed as failure rate in parts per million (ppm), for the whole lifetime.

Table 32 100% Lifetime Exposure to Overload (100% Duty Cycle)

Class	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V
FADC / Digital Input	0	0	0	2e-8	2e-7	3e-6	4e-5
A1	0	0	0	1e-8	1e-7	2e-6	2e-5
A2, LVDS	0	0	0	4e-8	4e-7	5e-6	6e-5

Note: Failure rate for 50% and 10% lifetime exposure to overload at room temperature approaches 0.

1.5.2.2 Reliability at High Temperatures

The reliability data given in this document is calculated for one pin of each relevant class. The reliability of n pins is derived by multiplying the one-pin reliability with the number of pins under consideration, of each pad class separately. The High Temperature case is the worst case, although the PN-junction voltages at high temperatures are the lowest.

PN Junction Characteristics

The following table gives the PN-junction voltage current dependence for 125°C, different pin classes.

Table 33 PN-Junction Characteristics

Class	0.2 mA	0.5 mA	1 mA	3 mA
LVDS	3.93 V	4 V	4.05 V	4.3 V
Digital Only	3.93 V	4 V	4.05 V	4.25 V
FADC	3.93 V	4 V	4.05 V	4.1 V
A1	3.85 V	3.95 V	4 V	4.07 V
A2	3.66V	3.72 V	3.78 V	3.9 V

These pin overload voltages refer to the nominal power supply of V_{DDP} = 3.3V. The maximum values are obtained, at V_{DDP} = 3.47V, by adding 0.17V to the values above.

Reliability Characteristics, High Temperatures

The following tables give the reliability calculated for a single pin of each pad class, High Temperature, total life-time 24000h at 125°C junction temperature. The reliability is expressed as failure rate in parts per million (ppm), for the whole lifetime.

Table 34 100% Lifetime Exposure to Overload (100% Duty Cycle)

Class	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V
FADC / Digital Input	0.0001	0.0012	0.016	0.21	2.7	35	460
A1	0.00005	0.0006	0.008	0.1	1.3	17	220
A2, LVDS	0.00014	0.0018	0.024	0.31	4	53	690

Table 35 50% Lifetime Exposure to Overload (50% Duty Cycle)

Class	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V
FADC / Digital Input	0.00001	0.00012	0.0015	0.02	0.26	3.4	44
A1	0.000005	0.00006	0.0007	0.01	0.12	1.6	21
A2, LVDS	0.000013	0.00017	0.0022	0.03	0.38	5	65

Table 36 10% Lifetime Exposure to Overload (in case of an external error)

Class	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V
FADC / Digital Input	4e-10	5e-9	6e-8	0.0001	0.0011	0.014	0.2
A1	2e-10	3e-9	3e-8	0.00004	0.0005	0.007	0.1
A2, LVDS	5e-10	7e-9	1e-5	0.00012	0.0016	0.02	0.3

1.5.2.3 Reliability Calculation Method

For each application a list of pins /overload conditions must be generated. First, currents per pin class, duration and number of pins are defined. For example:

Table 37 Step 1

Class	Current [mA]	Voltage [V]	Duration [lifetime%]	Reliability [ppm]	No. of Pins
LVDS	0,5		50%		4
FADC	3		10%		3
A1	1		50%		5
A2	1		50%		10

Then, from the PN-junction characteristics table (for high temperature), the voltages are filled in.

Table 38 Step 2

Class	Current [mA]	Voltage [V]	Duration [lifetime%]	Reliability [ppm]	No. of Pins
LVDS	0.5	4	50%		4
FADC	3	4.1	10%		3
A1	1	4	50%		5
A2	1	3.78	50%		10

Then, from the reliability tables for 125°C, the appropriate reliability per pin is filled in.

Table 39 Step 3

Class	Current [mA]	Voltage [V]	Duration [lifetime%]	Reliability [ppm]	No. of Pins
LVDS	0.5	4	50%	0,03	4
FADC	3	4.1	10%	0,0011	3

Table 39 Step 3

Class	Current [mA]	Voltage [V]	Duration [lifetime%]	Reliability [ppm]	No. of Pins
A1	1	4	50%	0,01	5
A2	1	3.78	50%	0,00017	10

Last Step 4 consists of multiplying the reliability with the corresponding number of pins and summing the results. In this case:

Reliability [ppm] = 0.00017*10+0.01*5+0.03*4 =
= 0.0017 +0.05 + 0.12 = ca. 0.17 ppm

This calculation is done for 3.3 V nominal power supply, at 125°C. If the upper maximum power supply voltage of 3,47 V is taken into account, then 0.17 V should be added to the overload voltages in Step 2. The corresponding number would not correspond to the statistical reality, because most of the power supplies do not supply the maximum upper limit voltage (see General Recommendations - **Section 1.5.1.3**).

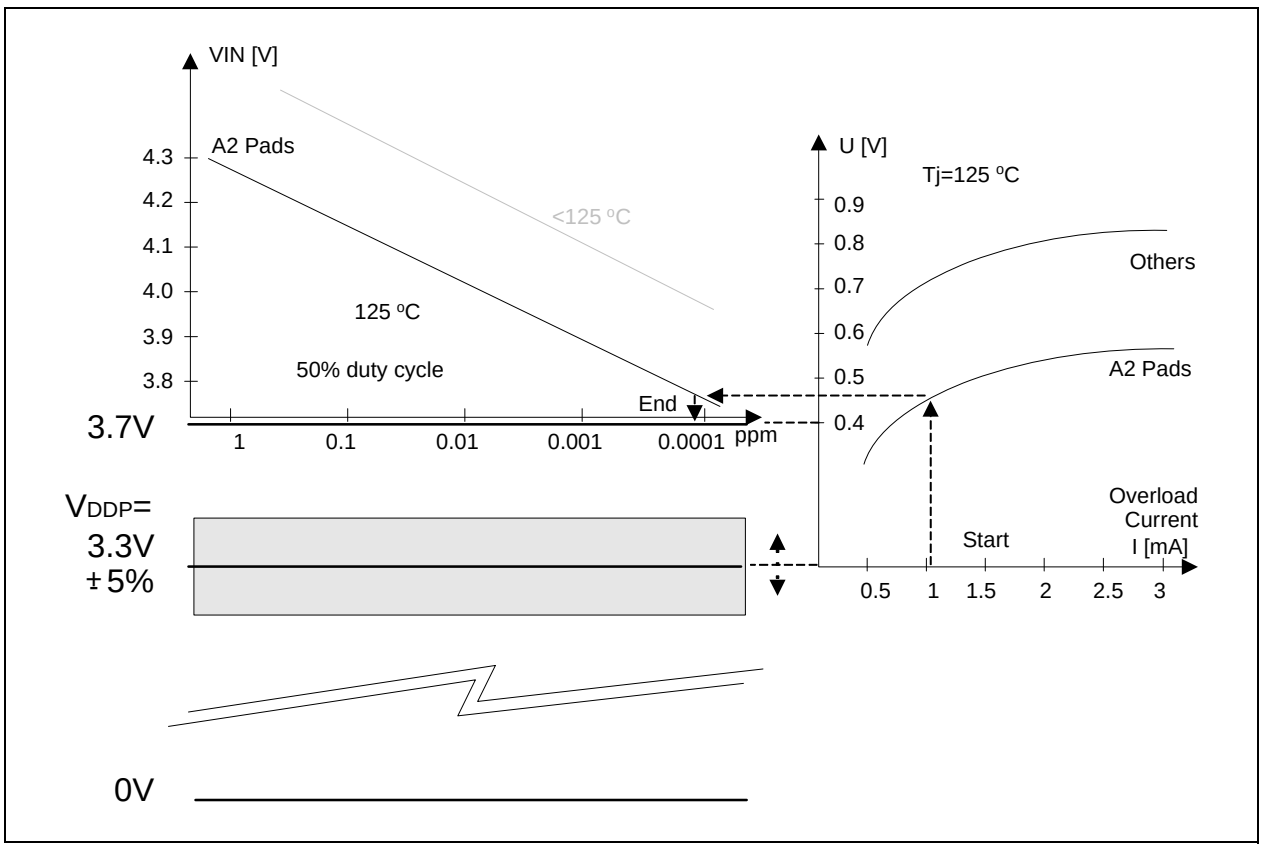


Figure 20 Graphical Representation of the Calculation Process

The **Figure 20** illustrates the concept behind the calculation. Starting point is the overload current, and the ending point is the ppm rate. The total overload voltage on a pin is a sum of the port supply voltage and the voltage of the protection diode in overload.

The **Figure 20** also shows that exceeding the 3.7 V on a pin leads to the necessity of calculating the failure rate in ppm, at high temperature and whole lifetime (50% duty cycle assumed). The **Figure 20** does not intend to describe accurately the physical laws and is not to be used as a calculation tool but only as an illustration. Calculations must be performed according to the described four steps procedure.

1.5.3 Negative Overload

The Negative Overload appears when the voltage on an input pin goes below the V_{SS}. The stress on some GOX surfaces is determined by the difference between the V_{DDP} power supply voltage and the voltage at the input pin. For example, if V_{DDP} = 3.3 V, and V_{IN} = -0.7 V, than the internal stressing voltage is equal to 4 V. Generally, this kind of stress influences fewer internal structures than the positive overload.

1.5.3.1 Reliability at High Temperatures

The reliability data given in this document is calculated for one pin of each relevant class. The reliability of n pins is derived by multiplying the one-pin reliability with the number of pins under consideration, of each pad class separately. The High Temperature case is the worst case, although the PN-junction voltages at high temperatures are the lowest.

PN Junction Characteristics

The following table gives the PN-junction voltage current dependence for 125°C, different pin classes.

Table 40 PN-Junction Characteristics

Class	-0.2 mA	-0.5 mA	-1 mA	-3 mA
LVDS / Digital Input	-0.31 V	-0.35 V	-0.4 V	-0.48 V
FADC	-0.31 V	-0.39 V	-0.4 V	-0.48 V
A1	-0.52 V	-0.61 V	-0.66 V	-0.73 V
A2	-0.29 V	-0.34 V	-0.38 V	-0.46 V

Adding 3.3 V to the absolute values from the table above gives the stressing voltage:

Table 41 Equivalent stressing voltage (3.3 V - U_{PN})

Class	-0.2 mA	-0.5 mA	-1 mA	-3 mA
LVDS / Digital Input	3.61 V	3.65 V	3.7 V	3.78 V
FADC	3.91 V	3.96 V	4.0 V	4.05 V
A1	3.82 V	3.91 V	3.96 V	4.03 V
A2	3.59 V	3.64 V	3.68 V	3.76 V

These pin overload voltages refer to the nominal power supply of V_{DDP} = 3.3 V. The maximum values are obtained, at V_{DDP} = 3.47 V, by adding 0.17 V to the values above.

Reliability Characteristics, High Temperatures

The following tables give the reliability calculated for a single pin of each pad class, High Temperature, total life-time 24000h at 125°C junction temperature. The reliability is expressed as failure rate in parts per million (ppm), for the whole lifetime. The data is related to the Negative Overload Condition, and Equivalent Stressing Voltage.

Table 42 Stress Voltage vs. Negative Overload Voltage for Vddp=3.3V

Overload	-0.4 V	-0.5 V	-0.6 V	-0.7 V	-0.8 V	-0.9 V	-1.0 V
Stress	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V

Table 43 100% Lifetime Exposure to Overload (100% Duty Cycle)

Class	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V
Digital Input	–	–	–	–	0.0003	0.002	0.009
FADC	–	–	–	–	–	–	–
A1	–	–	–	0.0002	0.0007	0.004	0.02
A2, LVDS	–	–	0.0002	0.0008	0.005	0.03	0.2

Table 44 50% Lifetime Exposure to Overload (50% Duty Cycle)

Class	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V
Digital Input	–	–	–	–	–	0.0004	0.002
FADC	–	–	–	–	–	–	–
A1	–	–	–	–	0.0002	0.0009	0.006
A2, LVDS	–	–	–	0.0002	0.001	0.007	0.04

Table 45 10% Lifetime Exposure to Overload (in case of an external error)

Class	3.7 V	3.8 V	3.9 V	4.0 V	4.1 V	4.2 V	4.3 V
Digital Input	–	–	–	–	–	–	0.0001
FADC	–	–	–	–	–	–	–
A1	–	–	–	–	–	–	0.0002
A2, LVDS	–	–	–	–	–	0.0003	0.002

The reliability calculation method for the negative overload is the same as for the positive overload.

1.5.4 FADC Input Buffer Reliability

The FADC input buffer is designed to operate within the normal operating conditions with input signals in 3.3 V range.

Overload condition can occur in the FADC if:

- A channel connected to 3.3 V input pad receives a voltage higher than the V_{DDMF} (3.3 V) supply voltage
- On an overlayed channel the FADC is enabled and the input signal is higher than V_{DDMF}

Overlayed FADC pins share the 5 V ESD protection with the ADC and non-overlayed FADC pins have their dedicated 3.3 V ESD protection.

All FADC input stages (double transmission gates) are protected with diodes against overvoltage.

The diodes limit the input voltage for all FADC inputs to 4.3 V.

Note: If an overload FADC channel is selected with a signal higher than V_{DDMF} +0.7 V the protection diode will clamp the input voltage to this level and cause additional leackage for the ADC input signal. This will increase the error of the ADC measurement.

1.5.5 LVDS / CMOS Combo Pad Reliability

The LVDS / CMOS combo pads are complex pads with relatively large stressed area, comparable to the stressed area of the A2 pads on one side, and UI characteristics of the ESD elements resulting in higher over-voltages on the other side. That makes them somewhat more sensitive to overload than the other digital pads. For the exact numbers, use the given values in the tables and the described calculation method.

1.5.6 Overload Electrical Parameters

Parameter	Symbol	Limit Values		Unit	Notes Conditions
		min.	max.		
Absolute Maximum Ratings					
Input current on any pin during overload condition[1)]	I_{IN}	-10	+10	mA	[2)]
Absolute maximum sum of all input circuit currents during overload condition[1)]	ΣI_{IN}	–	|100|	mA	[2) 3)]

1) This parameter is an Absolute Maximum Rating. Exposure to Absolute Maximum Ratings for extended periods of time may damage the device.

2) Refers to possibility of current caused degradation, where the voltages in overload do not violate the normal operating conditions. In case that the overvoltages violate the normal operating conditions, the reliability considerations caused by overvoltage apply independently, as described in this document.

3) Port Group restrictions apply.

Note: Under the following overload conditions at the digital GPIO pins:
-1 mA < IOV < 1 mA or
-3 mA < IOV < 3 mA, duration < 10% life-time 1)
and provided that the restrictions related to the sums of the overload/short-circuit currents for pin groups listed in the data sheet are met, there are no functional limitations imposed

Note: Under the overload conditions at all ADC analog pins:
-3 mA < I_{OV} < 3 mA, duration = 100% life-time
there are no reliability limitations and these pads are not discussed in this document. For the definition of the overload current I_{OV}, overload coupling factor k_{OV}, and all other details regarding the analog pins, see the general electrical specification.

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